AUDIO RINGING CODEC FILTER

PSB 2160
CONTENTS

Symbols

A/D	Analog to digital converter
ADI	ARCOFI digital interface
AFE	Analog front end
ALS	Analog loop back via converter register (CR1)
ALM	Analog loop back via MUX
AM	Address mode bit (CR2)
ARCOFI	Audio ringing codec Filter
ASP	ARCOFI signal processor
A/μ	A-Law/μ-Law bit (CR1)
CCITT	International Telegraph and Telephone Consultative Committee
CMDR	Command register
COP	Command operation
CR1-4	Configuration register 1-4
CRAM	Coefficient RAM
D1-D3	Decimation filter 1 to 3
D/A	Digital to Analog Converter
DLS	Digital loop back via Converter (CR1)
DLP	Digital loop back via PCM register (CR1)
DRAM	Data RAM
DSP	Digital signal processing
DTMF	Dual tone Multi-Frequency
ELS	Expansion Bit (CR2)
EFC	Enable feature control bit (CR2)
EWDF	Electric wave digital filter
FMH	Free hand microphone input pin
FR	Frequency correction receive bits (CR1)
FSC	Frame synchronization (8Khz)
FX	Frequency correction transmit bits (CR1)
GNDA	Analog ground (0V)
GNDD	Digital ground (0V)
GR	Receiver gain (CR1)
GX	Transmitter gain (CR1)
GZ	Side tone gain (CR1)
HFS	Hands-Free state (CR3)
HOP	Handset earpiece output + pin
HON	Handset earpiece output - pin
IDR	Initiallize Data RAM (CR1)
IOM	ISDN oriented modular
ISDN	Integrated service digital network
LSN	Loudspeaker output - pin
LSP	Loudspeaker output + pin
MIP	Handset microphone input + pin
MIN	Handset microphone input - pin
NOP	Normal operation
NOT	No test mode (CR1)

PCI	Peripheral Control Interface
POR	Power on reset
PU	Power up bit (CMDR)
RCS	Receive channel select bit (CMDR)
RDY	Ready state (CR3)
RX	Receive
SA-SD	PCI I/O Pins
CK	System clock pin (512Khz)
SIP	Serial interface port pin
SIPR	Serial interface port register
SLD	Subscriber line data
SOP	Status operation
SP1-2	Supplementary function pins 1-2
TG	Tone generator (CR4)
TM	Tone mode bits (CR4)
TR	Three party conferencing (CR4)
TX	Transmit
WDF	Wave digital filter

INTRODUCTION

The PSB 2160 ARCOFI provides the subscriber with an optimized Audio, Ringing, Codec, Filter processor solution for a digital telephone. The ARCOFI fulfils all necessary requirements for the completion of a low cost digital telephone. Full featured applications including hands free telephony are included by the addition of a voice switched speakerphone circuit. The ARCOFI performs all coding, decoding and filtering functions according to CCITT and AT&T norms.

The ARCOFI integrates a DTMF generator in the transmit direction and a tone generator plus a ringing generator in the receive path. The interfacing to a handset mouth and earpiece is facilitated by a flexible analog front end. A loudspeaker output has also been integrated on chip as well as a secondary input for a handsfree microphone. The microphone analog gains is user programmable under microprocessor control.

1. GENERAL DESCRIPTION

1.1 DISTINCTIVE FEATURES

* Applications in digital terminal equipment including a voice path
* Low power CMOS technology
* Test and maintenance loopbacks in the analog front end and the digital processor
* SLD or IOM(TM) Rev2 serial interface bus
* Flexible Peripheral Control Interface (PCI).
* CODEC filter
* DTMF, tone and ringing generators
* Separate output for a piezo ringer
* Dual analog inputs for handset and "handsfree" microphones plus an auxiliary differential analog input.
* Two sets of differential outputs for a handset earpiece and a loudspeaker
* Power dissipation: active 150 mw, standby 10 mw
* Temperature range: -25 to 70 C
* Package: 24 pin DIL

1.2 FUNCTIONAL DESCRIPTION

The ARCOFI bridges the gap between the audio world of microphones, earphones, loudspeakers and the PCM digital world by providing a full PCM CODEC (coder + decoder) with all the necessary transmit and receive filters. A block diagram of the ARCOFI is shown in FIG 1.2.1.

The ARCOFI can be subdivided in three main blocks;

* The ARCOFI Analog Front End (AFE)
* The ARCOFI Signal Processor (ASP)
* The ARCOFI Digital Interface (ADI)

A brief description of each block will provide acquaintance with the ARCOFI. A detailed description follows in the proceeding chapters.

1.2.1 ANALOG FRONT END (AFE)

The AFE interfaces the analog transducers i.e microphones, earpiece and loudspeaker to the ARCOFI.

The transmit section of the AFE consists of a high sensitivity differential input for a handset microphone, a differential auxiliary input and a single ended low sensitivity input for a handsfree microphone. Input sources are selectable via the analog I/MUX

The AFE receive direction features a handset earpiece differential output and a loudspeaker differential output. All outputs are selectable via the analog O/MUX.

High performance A/D and D/A converters provide the necessary interfaces with the ARCOFI signal processor section.

FIG 1.2.1 ARCOFI BLOCK DIAGRAM

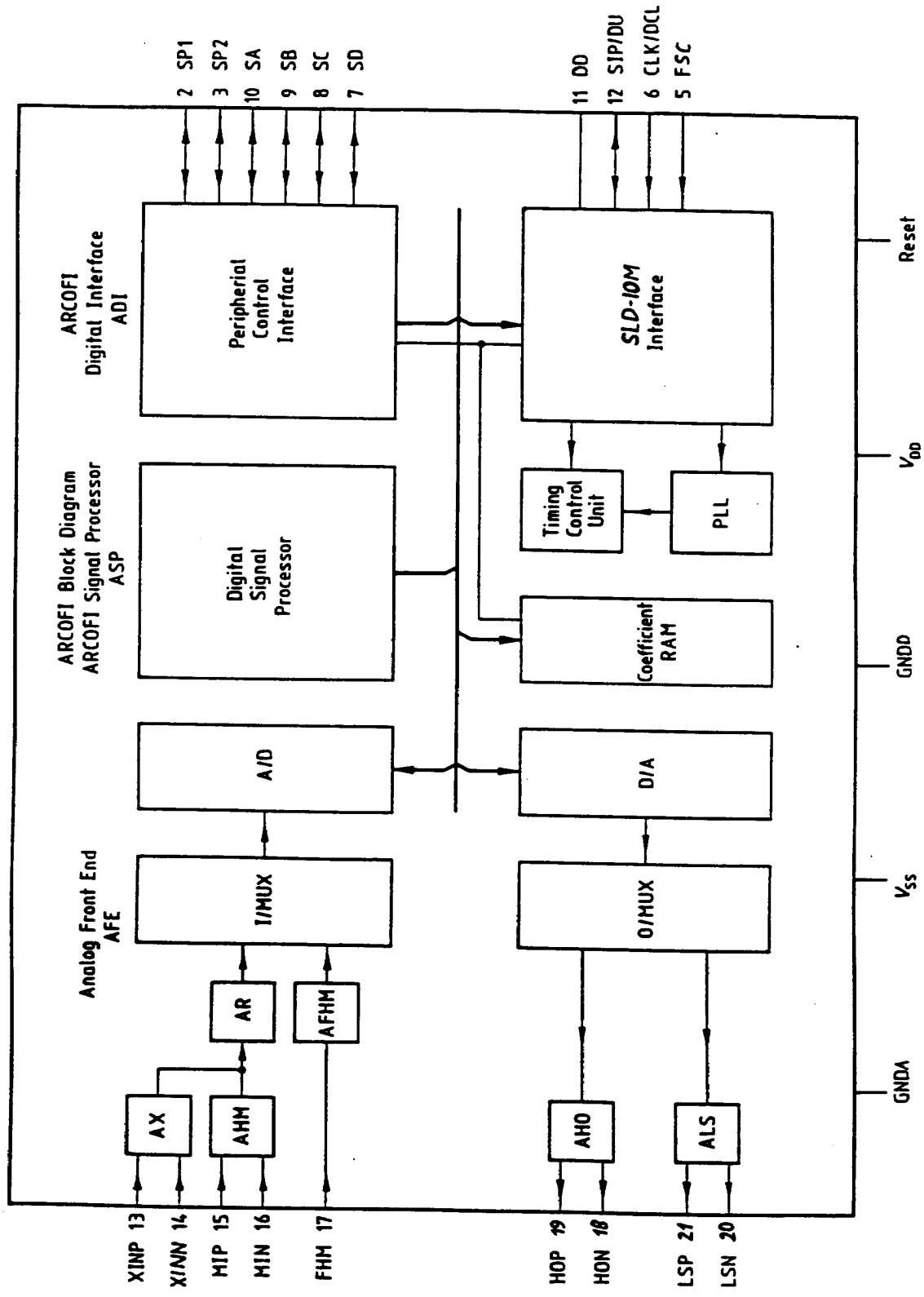
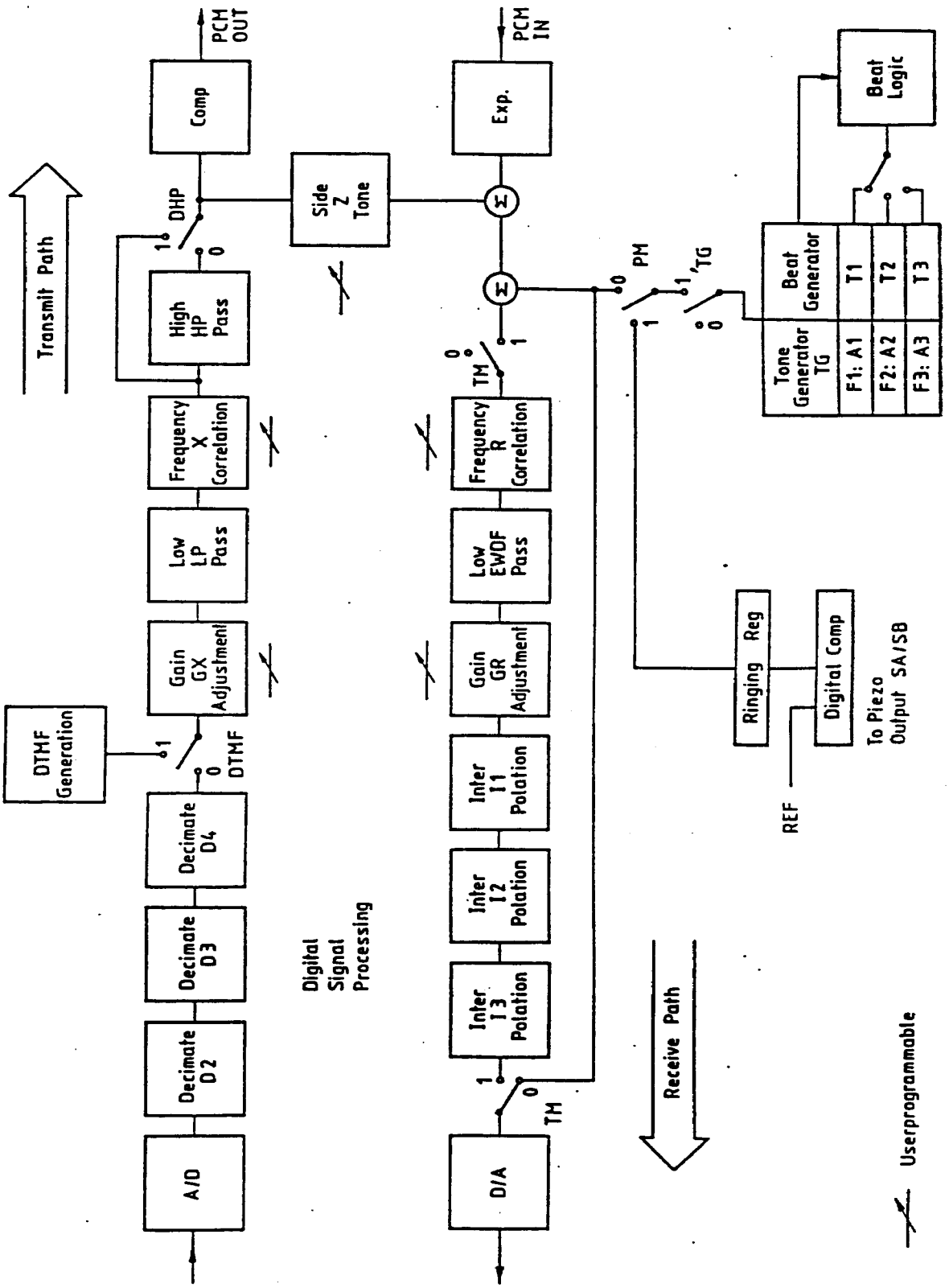


FIG 1.2.2 ARCOFI SIGNAL FLOW GRAPH



1.2.2 ARCOFI SIGNAL PROCESSOR (ASP)

The ASP block performs all the CODEC filter functions using digital signal processing techniques. All functions performed by the ASP section can be characterized by their high level of flexibility and programmability.

The ASP main features are:

* two gain adjustment stages

Gain adjustment for both receive and transmit path. A wide control range is programmable directly by the user. Transmit and receive level adaptation is therefore made possible.

* Two transducer correction filters

The FX filter in the transmit direction and the FR filter in the receive direction can be programmed to correct for the analog transducer frequency characteristics.

* Side tone gain adjustment

The side tone level can be adjusted via a programmable Z gain stage

* DTMF, ringing and tone generation

DTMF signals can be added in the transmit path. In the receive direction a multi tone ring signal can be generated and outputed by the loudspeaker or by an independent piezo ringer. Tones can also be superimposed on the incoming PCM signal. All tones are amplitude and frequency programmable.

1.2.3 ARCOFI DIGITAL INTERFACE (ADI)

The ADI features are:

* a selectable SLD or IOM(TM) Rev2 serial bus interface through which the ARCOFI transfer the voice channels and communicates with the system microcontroller

* A programmable multipurpose interface for Peripheral Control use (PCI). The PCI Interface provides 4 programmable I/O pins to control peripheral devices.

1.3 TYPICAL APPLICATION

The following diagrams illustrate some of the typical applications possible with the PSB 2160 ARCOFI.

1.3.1 ISDN IOM architecture (FIG 1.3.1)

This figure shows the ISDN oriented modular (IOM) architecture concept. In this context, the ARCOFI forms, together with the PEB 2070 ICC and a PEB 2080 SBC, or an ISAC-S PEB 2085 a complete digital telephone as specified in the CCITT I-series recommendation at the "S" reference point. The ARCOFI can also be used with the ISDN echo cancellation circuit PEB 2090 IEC to form a digital telephone at the "U" reference point. Other line transceiver such as the PEB 2095 ISDN Burst transceiver can also be used.

1.3.2 Digital feature phone (FIG 1.3.2)

The following example shows a typical digital feature phone application. The SAB 8051 microcontroller handles the key monitoring and display activities as well as some of the communication protocols (LAPD).

1.3.3 Digital feature phone with speakerphone (FIG 1.3.3)

A digital feature phone using the ARCOFI can easily be expanded for handsfree applications by the addition of a voice switched speakerphone circuit.

FIG 1.3.1 IOM ARCHITECTURE

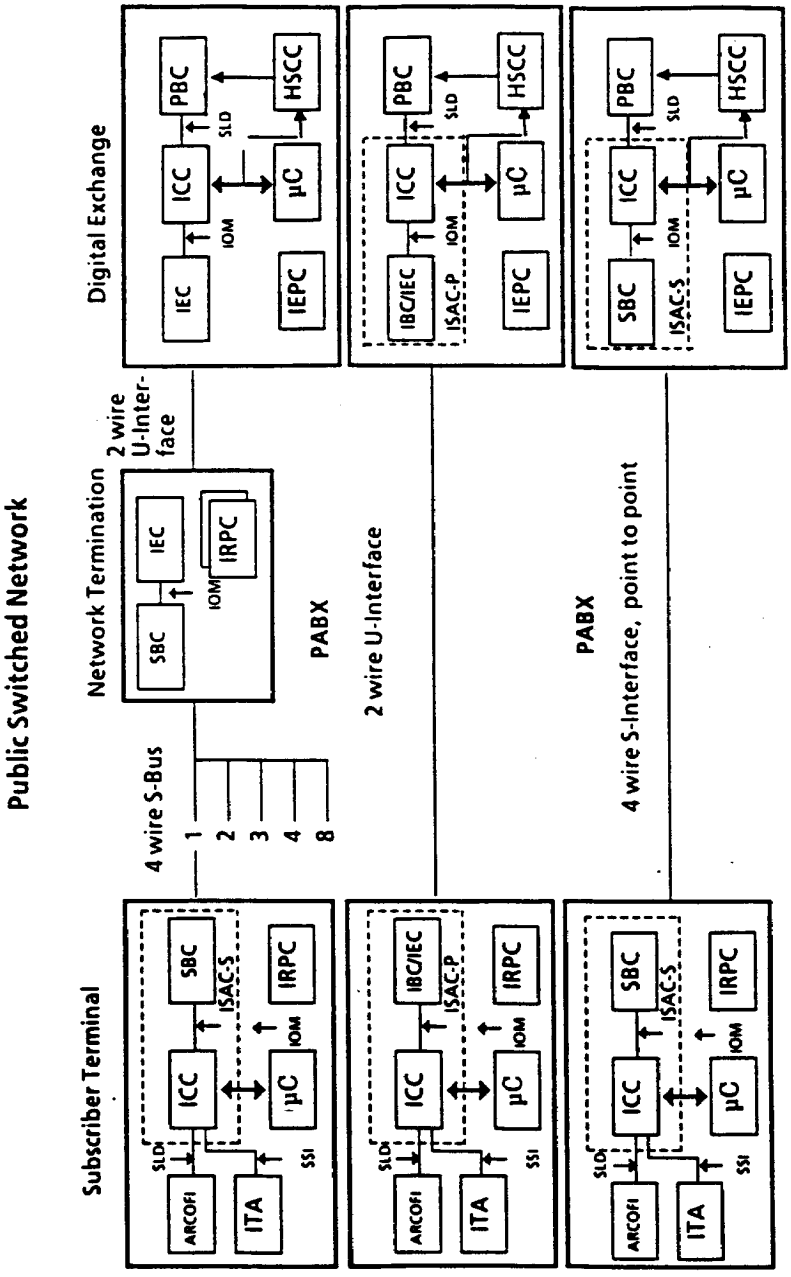


FIG 1.3.2 DIGITAL FEATURE PHONE

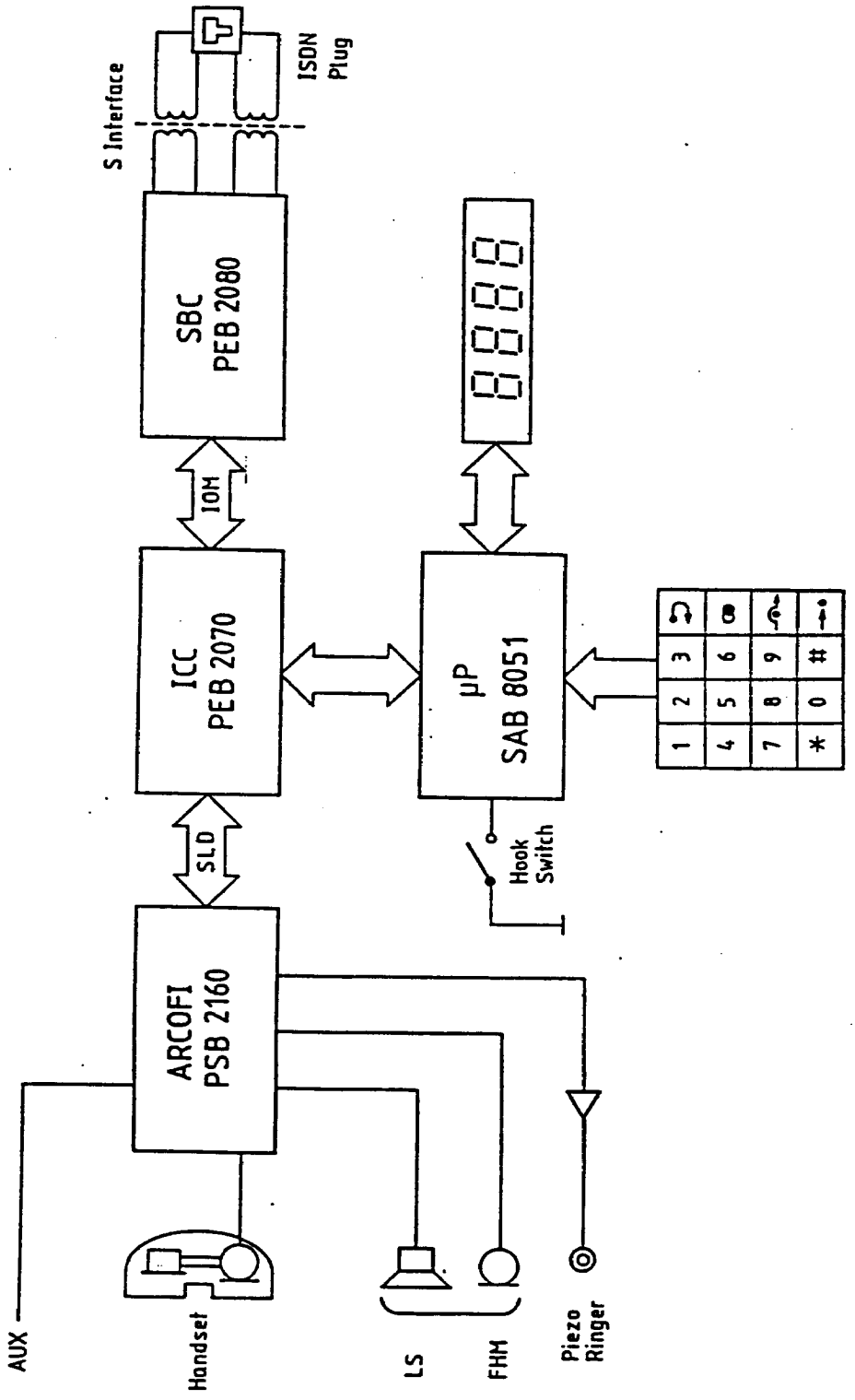
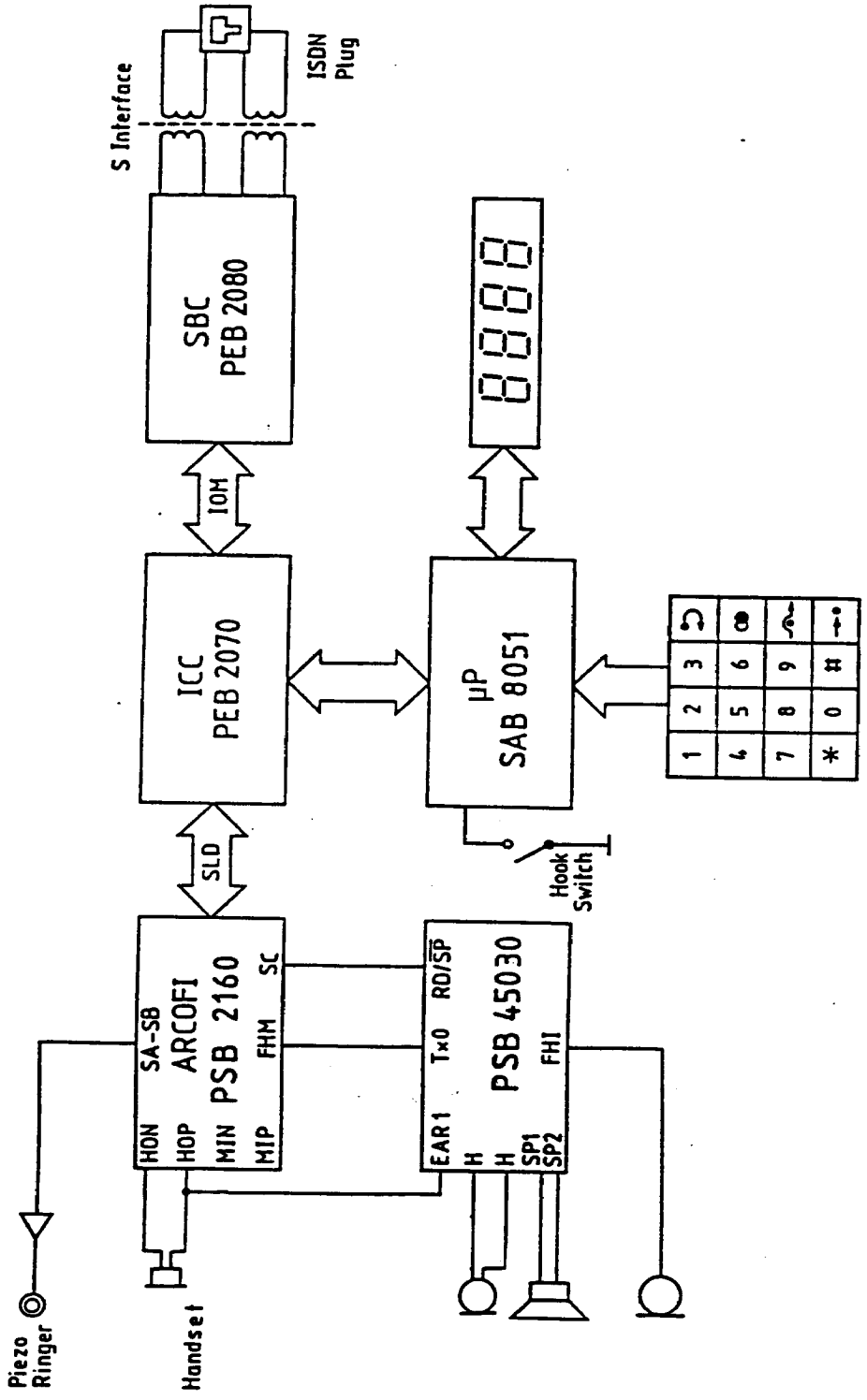


FIG 1.3.3 DIGITAL FEATURE PHONE WITH SPEAKERPHONE

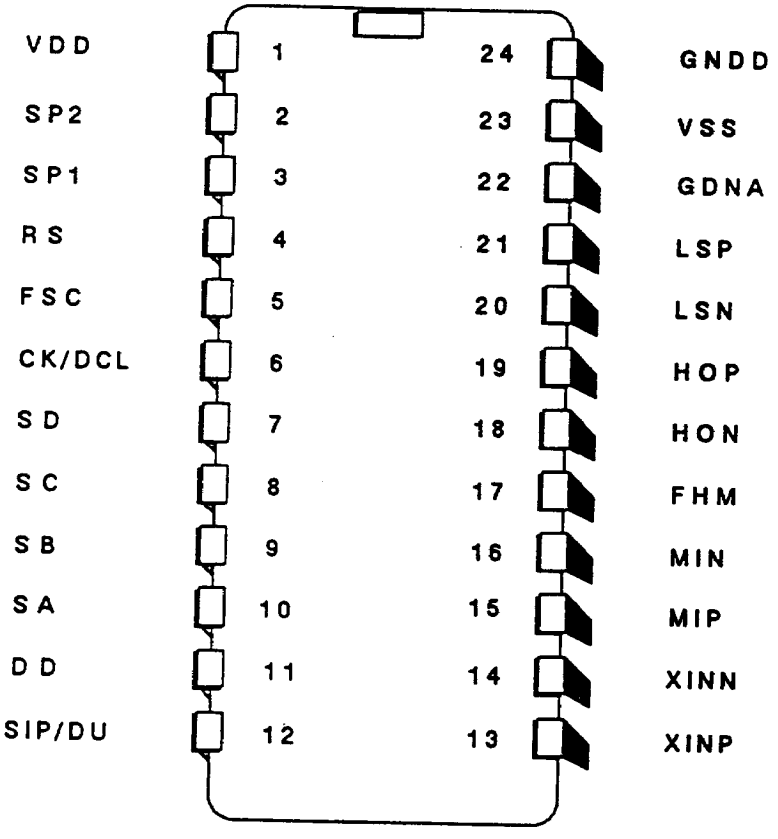


1.4 PIN DEFINITION & FUNCTIONS

PIN	SYMBOL	FUNCTION
1 23	**VDD** **VSS**	+5V Positive power supply -5V Negative power supply
22	**GNDA**	**Analog ground:** not internally connected to GNDD. All analog signals are referred to this pin
24	**GNDD**	**Digital ground:** (0V) not internally connected to GNDA. All digital signals are referenced to this pin
6	**CK/DCL**	**CK System clock:** 512 Khz supplied by the application system clock when SLD mode is selected. **DCL system clock:** 1.536 MHz supplied by the application system clock when IOM(TM) Rev2 mode is selected.
5	**FSC**	**Frame sync.:** 8khz signal, phase locked to CK. When high, SIP behaves as an input and the ARCOFI can receive data through pin SIP. When low, SIP behaves as an output and data can be transferred from the ARCOFI to the system via pin SIP. When in IOM(TM) Rev2 mode FSC supplies to the ARCOFI a synchronization signal according to the IOM(TM) Rev2 specification.
12	**SIP/DU**	**SIP; Serial Interface Port:** This serial bidirectional port is clocked by CK when SLD mode is selected. **DU; data upstream:** Transmit data to the layer 1 IOM(TM) Rev2 controlling device.
11	**DD**	**DD; Data Downstream:** Receive data from a layer 1 IOM(TM) Rev2 controlling device.
7 8 9 10	**SD** **SC** **SB** **SA**	**Programmable I/O PCI pins:** With the appropriate bit setting in configuration register CR2, each SA-SD pin can be declared independently an input or an output. Data received or forwarded to the PCI pins are allocated to the signalling channel. When selected, the tone generator signals can be directed to pins SA & SB. (SA & SB then in opposite phase).

PIN	SYMBOL	FUNCTION
3 2	**SP1** **SP2**	**Supplementary function:** Appropriate pin strapping access Supplementary functions including test modes as described in section 4.0 ADI.
4	**RS**	**Reset input:** When pin RESET is forced high the ARCOFI is placed in a power down mode. All configuration registers are reset to default values. I/O pins SA-SD and SIP/DU are defaulted to inputs until the ARCOFI is reconfigured
16 15	**MIN** **MIP**	**Handset microphone inputs:** MIP & MIN provides highly symmetrical differential inputs for commonly used telephone microphones.
17	**FHM**	**Freehand microphone:** This single ended input can be used to interface an electret microphone for speakerphone applications.
14 13	**XINN** **XIN**	**X input:** These auxiliary inputs provides a normalized differential audio input for an additional analog device.
21 20	**LSP** **LSN**	**Loudspeaker outputs:** LSN and LSP are differential outputs pins which can drive a 50 Ohms loudspeaker directly. A piezo transducer connected via SA and SB can also be used for ringing signals instead of a loudspeaker
19 18	**HOP** **HON**	**Handset earpiece outputs:** HOP & HON are differential output pins which can drive handset earpiece transducers directly

FIG 1.4.1 ARCOFI PINOUT



1.5 PROGRAMMABLE REGISTERS

The SLD or the IOM(TM) Rev2 bus mode is used to control and program the operations performed by the ARCOFI. The following lists the ARCOFI internal registers as they appear in each section.

ARCOFI DIGITAL INTERFACE (ADI)

* CMDR: 8 bit command register
* CR1-4: four 8 bits configuration registers
* SIPR: 8 bits serial interface port register
* PCIR: 4 bits peripheral control register
* PCMR1-2; Two 8 bits PCM registers

ARCOFI SIGNAL PROCESSOR (ASP)

* Two transmit gain registers
* Two receive gain registers
* 10 FX filter coefficient registers
* 10 FR filter coefficient registers
* One Z sidetone gain register
* Two DTMF frequency tone registers
* 6 Tone Ring/Tone Generator frequency register
* 3 Tone Ring/Tone Generator amplitude register
* 6 Beat tone Generator timing register

1.6 OPERATING MODES

Some of the possible ARCOFI operating modes are documented in the proceeding paragraph. The four ARCOFI configuration registers have enough built in flexibility to accommodate an extensive set of user calling procedures. In conjunction with the system µP, the PEB 2070 ICC ISDN communication controller and the PEB 2080 SBC S-Bus Controller, the system designer can implement an extensive set of terminal attributes.

The following operating mode description table is not exhaustive but should be used as an example of possible functions performed by the ARCOFI.

OPERATING MODES

STATE	DESCRIPTION
POR	Power on reset: When power is supplied to the ARCOFI a hardware reset via an RC network connected to input pin RESET will force all ARCOFI internal registers to default values. The ARCOFI registers reset state is described in section 4.0 (ADI)
STAND BY	The system microprocessor can initiallize the ARCOFI via the SLD or the IOM(TM) Rev2 bus to a different set of filter and configuration values. Whilst remaining in power down (PU=0,CMDR) a new set of filter coefficient and configuration bits can be loaded in the ARCOFI.
READY	The system MPU detects activity from the hook-switch or from the keyboard. The ARCOFI can be placed in READY state where all handset I/O are enabled (MIP,MIN & HOP,HON activated).
RINGING	The system MPU detects an incoming call, the ARCOFI can be placed in a RINGING state by activating the tone ringer via CR4 and configuring the ARCOFI such that either the loudspeaker outputs LSN & LSP or the piezo ringer outputs pin SA & SB are enabled.
DTMF	All audio inputs can be disabled by forcing a MUTE code in CR3. DTMF tones are generated in the ASP transmit path.

OPERATING MODES CONT'D

STATE	DESCRIPTION
PULSE DIAL	Handset audio path can be enabled by forcing a READY code in CR3. A single tone can be superimposed into the audio receive path so as to provide audible feedback when dialling.
LOUD HEARING	The handset microphone inputs MIP & MIN and the loudspeaker outputs LSN & LSP can be activated by configuring CR3.
HANDS FREE	The handset audio I/O's are disabled. The handsfree microphone input and loudspeaker outputs LSN & LSP are activated by configuring CR3.
MUTE	The ARCOFI can be placed in a mute state by enabling the handset outputs HOP & HON. All other analog I/O's being disabled. (MUTE code in CR3).
FEATURE TONE	A single tone can be superimposed to the incoming PCM voice signal. Application requiring system function audible feedback are therefore made possible.

2. ANALOG FRONT END DESCRIPTION

The analog front end section of the ARCOFI interfaces the analog transducers with the subsequent signal processor. In the transmit direction the AFE function is to amplify the transducer input signals (microphones) and convert them into digital signals. In the AFE receive section , the incoming digital signals are converted to analog outputs so as to drive an earpiece and a loudspeaker. The attenuation plan and electrical characteristics of the AFE are adapted to meet commonly used voice transducers.

2.1 ANALOG INPUTS

A high sensitivity differential input MIP and MIN connects a handset microphone to a gain programmable amplifier Ahm. When selected the differential X inputs can be activated while deselecting the MIP/MIN inputs; a fixed amplification stage AX connects point 2.1 to the input of the analog multiplexer driving the oversampling A/D converter. A third analog input source is provided through pin FHM. This "handsfree" microphone input connects the multiplexer via amplifier Afhm. The programmable amplifier Ahm provides a coarse gain adjustment range, thus allowing a perfect adaptation to various types of microphone transducers. Fine gain adjustment is performed in the digital domain via the programmable gain adjustment filter GX (see ARCOFI signal processing section). The main electrical characteristics of the analog inputs are summarized in table 2.3.1

2.2 ANALOG OUTPUTS:

Fully differential outputs HOP and HON connect the amplifier Aho to the handset earpiece. Differential outputs LSN & LSP are provided for use with a 50 ohm loudspeaker. Up to 100 mW of power can be delivered to the loudspeaker via amplifier Als. The Als power amplifier Als is short circuit protected. All outputs are sourced by a digital to analog converter via an output analog multiplexer. The selection of the output source is performed through the configuration register CR3 via the SLD interface. The main electrical characteristics of the analog outputs are summarized in table 2.3.2

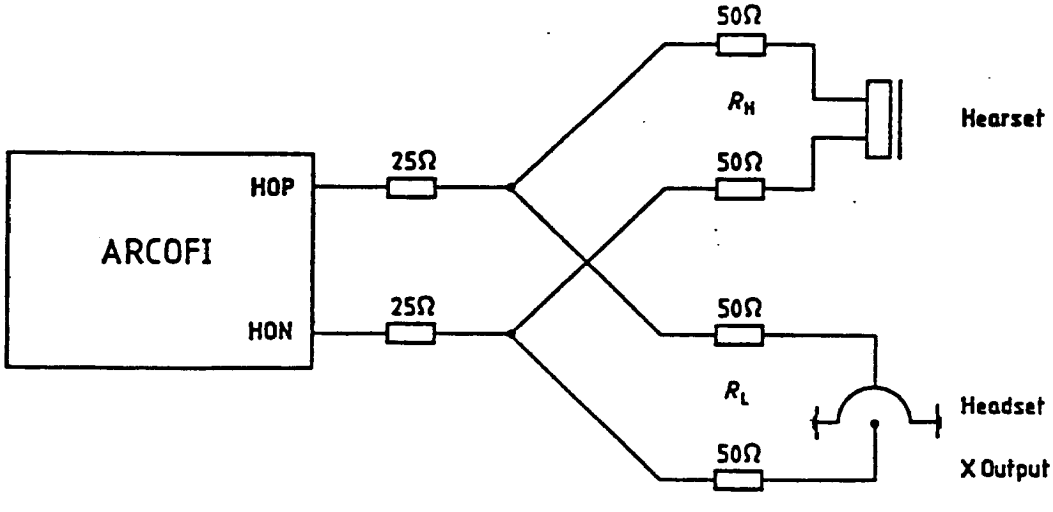
2.2.1 AUXILIARY OUTPUT

A separate auxiliary X output can be provided in conjunction with the hearpiece output. The discrete circuit diagram shown in FIG 2.2.1 is suggested when an auxiliary head set output is required. Table 2.2.1 indicate the resulting output levels for different load impedances.

TABLE 2.2.1

OUTPUT LOAD IMPEDANCE		IDLE	MIN	TYP	MAX	UNIT	REF
RL	RH	0.00	2.54E-02	1.43E-01	8.03E-01	Vpk	v
			1.80E-02	1.01E-01	5.68E-01	Vrms	v
10KΩ	>10KΩ		-39.00	-24.00	-9.00	dBmO	1.6 v
			-32.70	-17.70	-2.70	dBm	0.775 v
Aho gain			-10.70	-10.70	-10.70	dB	gain
RL	RH	0.00	1.44E-02	8.12E-02	4.57E-01	Vpk	v
			1.02E-02	5.75E-02	3.23E-01	Vrms	v
200Ω	>10KΩ		-43.90	-28.90	-13.90	dBmO	1.6 v
			-37.60	-22.60	-7.60	dBm	0.775 v
Aho gain			-15.60	-15.60	-15.60	dB	gain
PCM VALUE		+/-0	+/-43	+/-83	+/-123	PCM	code

FIG 2.2.1 AUXILIARY OUTPUT



2.3.1 ANALOG FRONT END ELECTRICAL INTERFACE INPUTS

TABLE

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST COND
ZHM	Handset microphone input impedance	10		Kohm	300-3400Hz
VHM	Handset microphone max input voltage swing 1)		7.58	mVpk	
Ahm +Ar	Handset microphone amplifier gain Ahm+Ar	0	51.2	dB	Pin MIP,MIN 1.35 mV @ 1Khz
ZFHM	Handsfree microphone input impedance	10		Kohm	300-3400Hz
VFHM	Handsfree microphone max input voltage swing 1)		110	mVpk	
Afhm	Handsfree microphone amplifier gain		28.0	dB	Pin FHM 19.5 mV @ 1Khz
ZXIN	Auxiliary pin input impedance	10		Kohm	300-3400Hz
VXIN	Auxiliary Xin max input voltage swing 1)		531	mVpk	
Axin	Auxiliary Xin amplifier gain Ax+Ar		15.1	dB	Pin XINN & XINP 110 mV @ 1Khz

1) A maximum swing signal correspond to a 3 dBm0 signal at the A converter which translate into a PC= code overload (+/-127) (3 d = 2.26 Vrms = 3.196 Vp= 6.392 Vpp)

2.3.2 ANALOG FRONT END ELECTRICAL INTERFACE OUTPUTS

TABLE

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST COND
ZHO	Handset earpiece output impedance		1	Ohms	300-3400Hz
VHO	Handset earpiece max output voltage swing 1)		457	mVpk	Load measured from HOP to HON
VHOH	Handset earpiece output high voltage 1)			V	input load -100mA @ HOP/HOP
VHOL	Handset earpiece output low voltage 1)			V	input load +100mA @ HOP/HOP
ZLS	Loudspeaker output impedance		2	Ohms	300-3400Hz
VLS	Loudspeaker max output voltage swing 1)		2.75	Vpk	Load measured from LSN to LSP
VLSOH	Loudspeaker output high voltage 1)			V	input load -100mA @ LSN/LSP
VLSOL	Loudspeaker output low voltage 1)			V	input load +100mA @ LSN/LSP

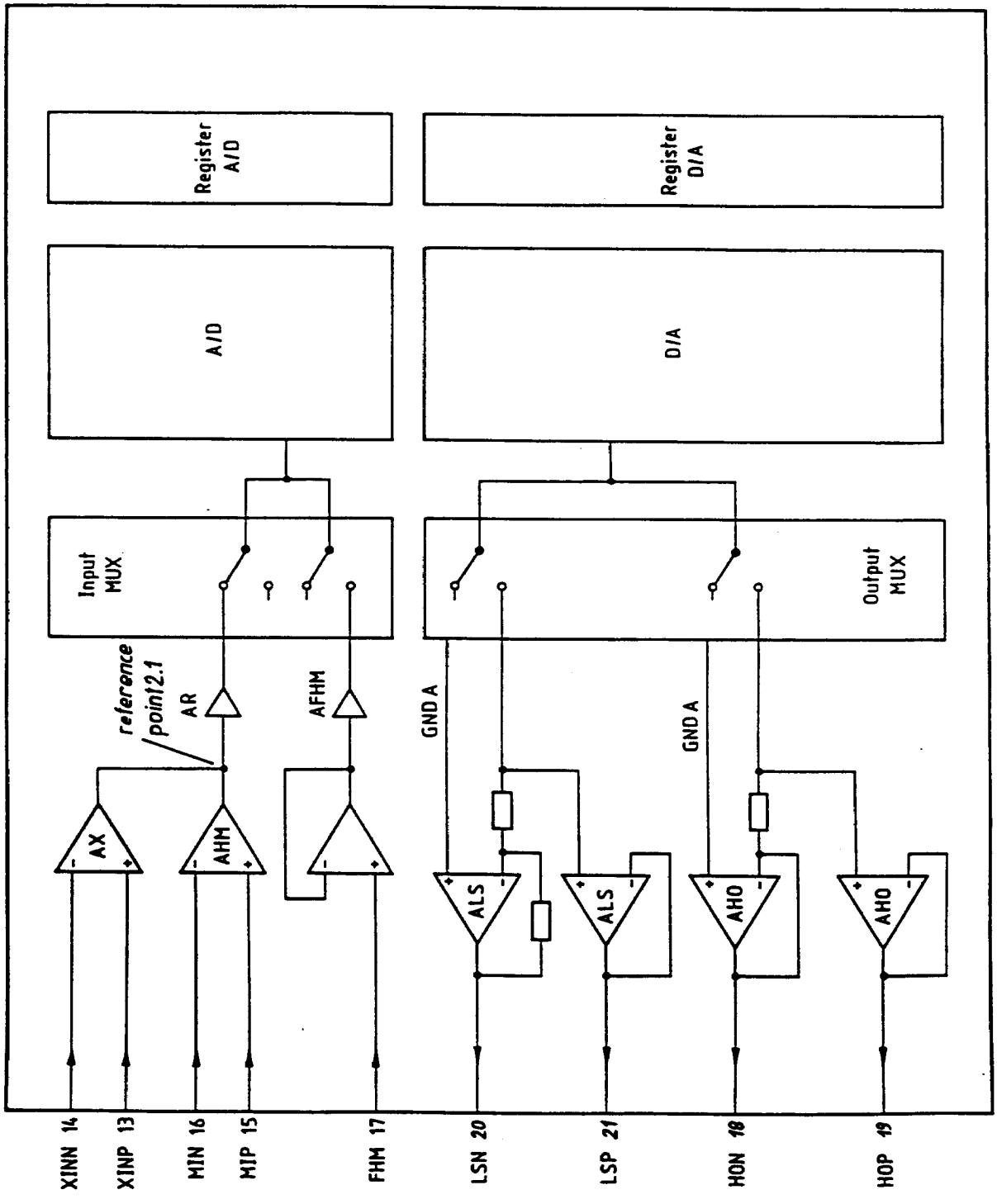
1) The max output voltage swing correspond to a max incoming PCM code (+/-127).

2.3.3 ARCOFI AFE ATTENUATION PLAN

TRANSMIT	IDLE	MIN	TYP	MAX	UNIT	REF
MIP/MIN GRAY MICROPHONE INPUT LEVEL	0.00	2.40E-04 1.70E-04 -79.50 -73.20	1.35E-03 9.53E-04 -64.50 -58.20	7.58E-03 5.36E-03 -49.50 -43.20	Vpk Vrms dBmO dBm	 1.6 0.775
Ahm+Ar gain		51.20	51.20	51.20	dB	gai
XIN INPUT LEVEL	0.00	1.68E-02 1.19E-02 -42.60 -36.30	9.44E-02 6.67E-02 -27.60 -21.30	5.31E-01 3.75E-01 -12.60 -6.30	Vpk Vrms dBmO dBm	 1.6 0.775
Ax+Ar gain		14.30	14.30	14.30	dB	gai
FHM INPUT LEVEL	0.00	3.47E-03 2.45E-03 -56.30 -50.00	1.95E-02 1.38E-02 -41.30 -35.00	1.10E-01 7.75E-02 -26.30 -20.00	Vpk Vrms dBmO dBm	 1.6 0.775
Afhm gain		28.00	28.00	28.00	dB	gai
A/D INPUT LEVEL ARCOFI =>	0.00	8.70E-02 6.15E-02 -28.30 -22.00	4.89E-01 3.46E-01 -13.30 -7.00	2.75E+00 1.95E+00 1.70 8.00	Vpk Vrms dBmO dBm	 1.6 0.775
PCM VALUE	+/-0	+/-43	+/-83	+/-123	PCM	codewor

RECEIVE	IDLE	MIN	TYP	MAX	UNIT	RE
D/A OUTPUT LEVEL ARCOFI =>	0.00	8.71E-02 6.15E-02 -28.30 -22.00	4.89E-01 3.46E-01 -13.30 -7.00	2.75E+00 1.95E+00 1.70 8.00	Vpk Vrms dBmO dBm	 1.6 0.775
LSN/LSP OUTPUT LEVEL IN A 50ohm LOAD ARCOFI => Als gain	0.00	8.71E-02 6.15E-02 -28.30 -22.00 .00	4.90E-01 3.46E-01 -13.30 -7.00 .00	2.75E+00 1.95E+00 1.70 8.00 .00	Vpk Vrms dBmO dBm dB	 1.6 0.775 gai
HON/HOP OUTPUT LEVEL hon=200Ω x=10KΩ Aho gain	0.00	1.44E-02 1.02E-02 -43.90 -37.60 -15.60	8.12E-02 5.75E-02 -28.90 -22.60 -15.60	4.57E-01 3.23E-01 -13.90 -7.60 -15.60	Vpk Vrms dBmO dBm dB	 1.6 0.775 gain

FIG 2.3.3 AFE BLOCK DIAGRAM



3. ARCOFI SIGNAL PROCESSOR DESCRIPTION (AFE)

3.1 THE ARCOFI SIGNAL PROCESSOR (ASP)

The ARCOFI signal processor (ASP) is programmed to perform all CCITT recommended filtering in both the transmit and receive path and is therefore fully compatible to the G.712 CCITT specification. The code processed by the ASP is provided in the transmit direction by an oversampling A/D converter situated in the analog front end (AFE). Once processed the speach signal is converted into an 8 bit A law or μ law PCM format or remains a 16 bit linear word according to the bit setting in the configuration register 3 (see CR3 in section 4.0, ADI).

In the receive direction the incoming PCM stream is expanded in a linear format and subsequently processed until passed to the D/A converter.

The entire ARCOFI signal flow plan is shown in FIG 3.1.1

3.2 TRANSMIT PATH SIGNAL PROCESSING

In the transmit direction series of decimation filters reduce the sampling rate down to the 8 kHz PCM rate. These filters attenuate out of band noise by limiting the received signal to the voiceband.

The decimation stages end with a low pass filter which band limits the voice signal according to the CCITT recommendation G.712. A high pass filter is also provided to remove power line frequencies. The ARCOFI meets or exceeds all CCITT, and north American recommendation on attenuation distortion and group delay distortion (See Fig 3.2.1 and 3.2.2)

The GX gain adjustment stage is digitally programmable allowing the gain to be programmed from -45 to +12 dB within a +/-0.25 dB tolerance range. Two bytes are necessary to set GX to the desired value.

The voice signal after being linearly processed can be outputed as an 8 bit PCM word according to the CCITT G711 A-LAW or the north American μ-Law format. If desired the compression stage can be by-passed, a 16 bits linear word is then outputed to the ARCOFI digital interface.

The transmit path contain a frequency correction filter FX allowing an optimum adaptation to different type of microphones (dynamic, Piezoelectric or electret).

The following parameters are specified for the transmit path. The measurements are made with GX and FX disabled and are applicable for both A-LAW or μ-LAW.

Fig 3.1.1 ARCOFI SIGNAL FLOW GRAPH

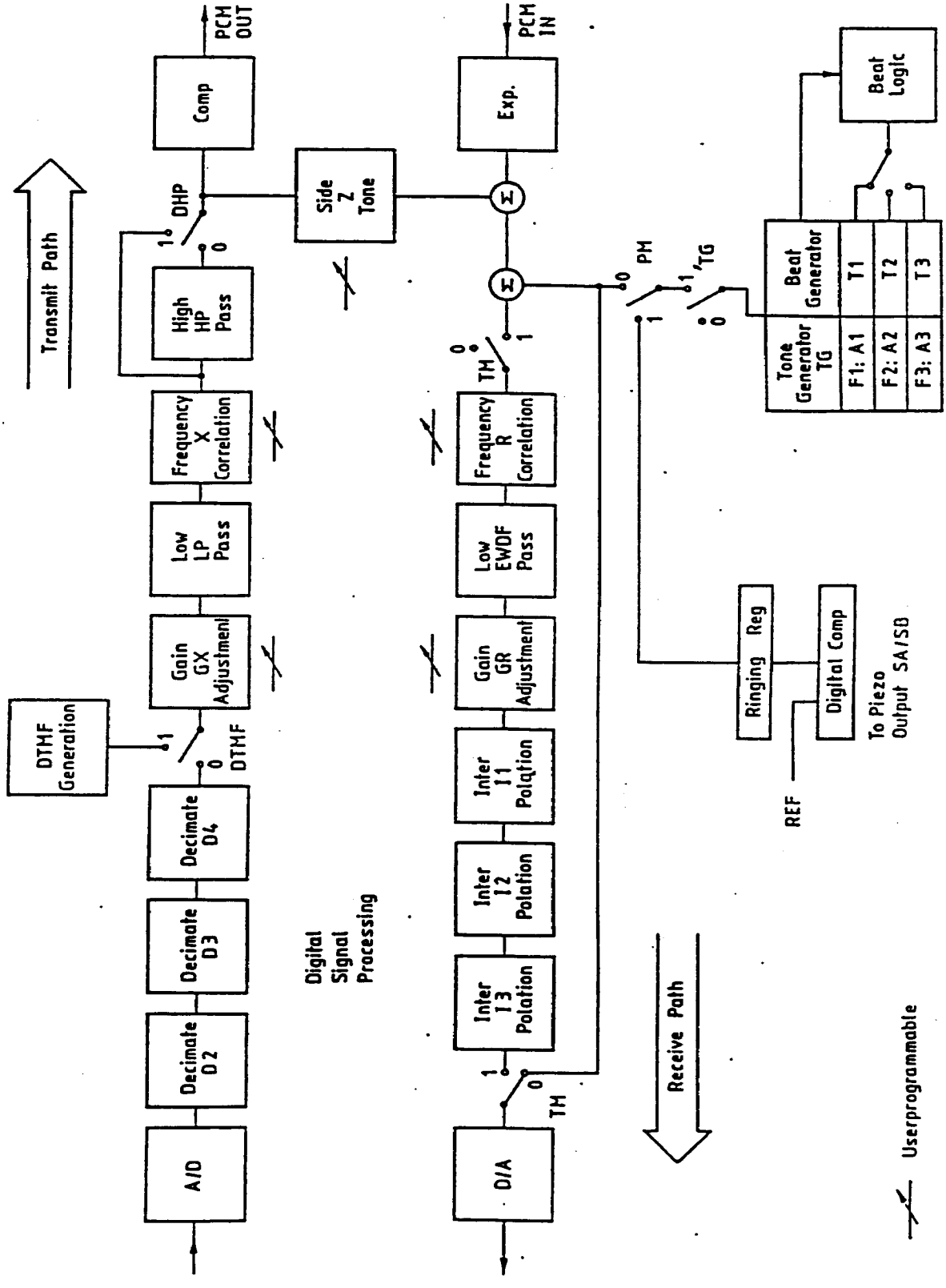


Fig 3.2.1 ATTENUATION DISTORTION IN TRANSMIT DIRECTION

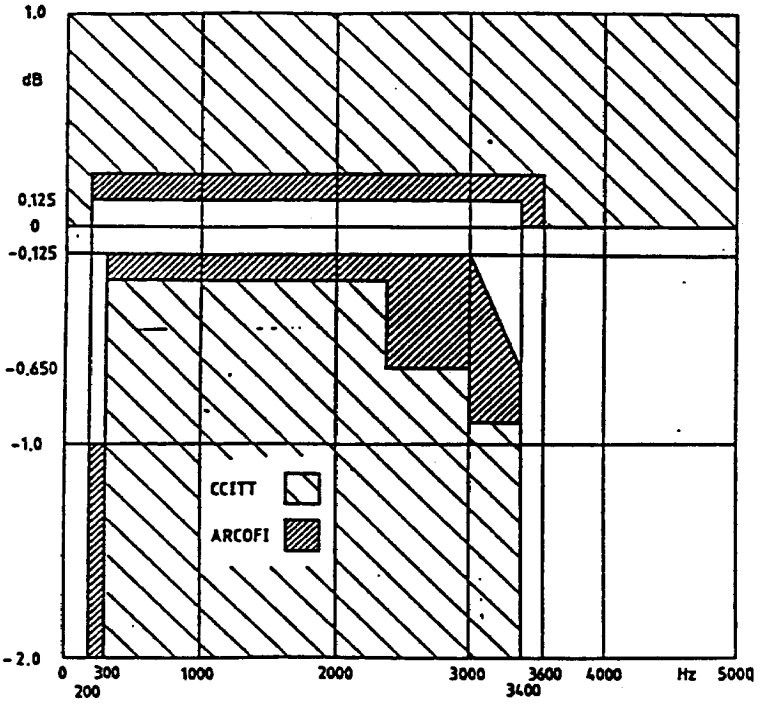
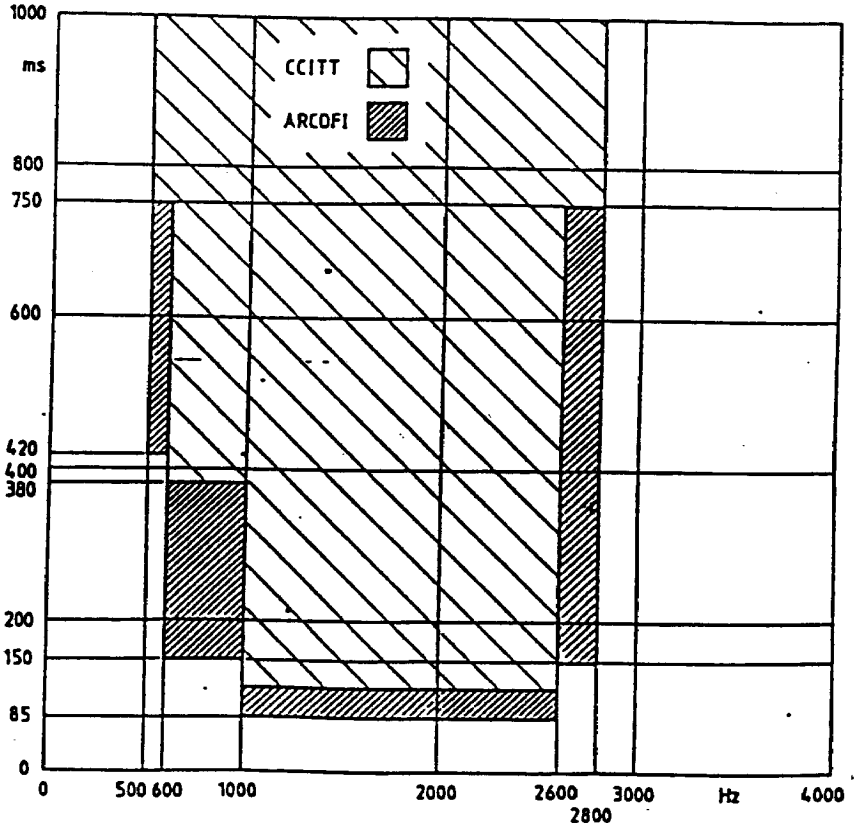


Fig 3.2.2 GROUP DELAY DISTORTION IN TRANSMIT DIRECTION



3.2.3 TRANSMISSION CHARACTERISTICS

PARAMETERS	TEST CONDITION	MIN	TYP	MAX.	UNITS
Gain	50/60Hz			-25	dB
relative	200Hz	-1.8			dB
to a 0dBmo	300-3000Hz	-0.5		0.5	dB
1000Hz signal	3400Hz	-1.8		0.5	dB
CCITT G712	4000Hz			-14	dB
Envelope 1)	500Hz			1.5	ms
delay distor-	600Hz			0.75	ms
tion @ 0dBmo	1000-2600Hz			0.25	ms
CCITT G712	2800Hz			1.5	ms
Gain traking	+3 to -40dBmO	-0.5		0.5	dB
CCITT	-40 to -50dBmO	-1		1	dB
method 2	-50 to -55dBmO	-3		3	dB
Quantization	0 to -30dBmO	33			dB
distortion	-40dBmO	27			dB
CCITT G712	-40dBmO	22			dB
method 2					
Idle channel	C-message			-22	dBmCO
noise	psophometric			-66	dBmOp

1)Delay measurements include delays through the A/D with all feature filters FX,GX disabled.

OUT-OF-BAND SIGNALS AT ANALOG INPUTS

When applying an out of band sine wave signal with frequency F and level A to the Analog inputs the level of any frequency component below 4kHz at the digital output is attenuated according to the following table.

The reference level used for this measurement is a 800Hz, 0dBmO signal applied to the FHM analog input in BY-PASS mode. The Digital gain GX in configuration register CR1 has to be set to a flat 0dB.

out-of-band input frequency F	out-of-band input level A	attenuation at digital output
0Hz <=F<= 60Hz	-45dBmO <=A<= 0dBmO	25dB
60Hz <=F<= 100Hz	-45dBmO <=A<= 0dBmO	10dB
3400Hz <=F<= 4000Hz	-45dBmO <=A<= 0dBmO	0dB
4000Hz <=F<= 4600kHz	-45dBmO <=A<= 0dBmO	14dB
4600Hz <=F<= 12kHz	-45dBmO <=A<= -15.8dBmO	35dB
12kHz <=F<= 20kHz	-45dBmO <=A<= -23.2dBmO	35dB
20kHZ <=F	-45dBmO <=A<= -25 dBmO	35dB

3.2.4 DTMF GENERATOR

A DTMF generator is also built into the ARCOFI transmit path. The DTMF generator is programmed by a COP command (see section 4.0 ADI). Two frequency values for the dual tones must be written into the coefficient RAM (COP_8 + 2 bytes) before activating the DTMF generator through a SOP_7 command (CR4, bit 6). The signal amplitude is programmed via the GX gain coefficient (COP_2 + 2 bytes)

A premphasis of 2 dB is guarantied between the high and the low DTMF frequency groups. The total power level of all unwanted frequency components is at least 20 dB below the level of the low frequency group component of the signal.

The level of any unwanted frequency component does not exceed the following limits:

- In the frequency band 0-300 Hz: > -33 dB
- In the frequency band 300-3,4 kHz: > -20 dB
- In the frequency band 3,4-4,0 kHz: > -33 dB

All generated DTMF frequencies are guarantied within a +/- 1% deviation. A typical DTMF programming sequence is highlighted in Fig 3.2.5

DTMF FREQUENCY PROGRAMMING

CCITT Q.23	ARCOFI NOMINAL	RELATIVE DEVIATION FROM CCITT *	HEX COEFFICIENT H nibble/L nibble
Low Group			
697	697.754	+ 1 081 ppm	F8
770	773.438	+ 4 464 ppm	A8
852	852.783	- 513 ppm	F9
941	939.453	- 1 646 ppm	BA
High Group			
1 209	1 203.125	- 4 883 ppm	21
1 336	1 339.844	+ 2 877 ppm	40
1 477	1 476.563	- 295 ppm	10
1 633	1 632.813	- 114 ppm	00

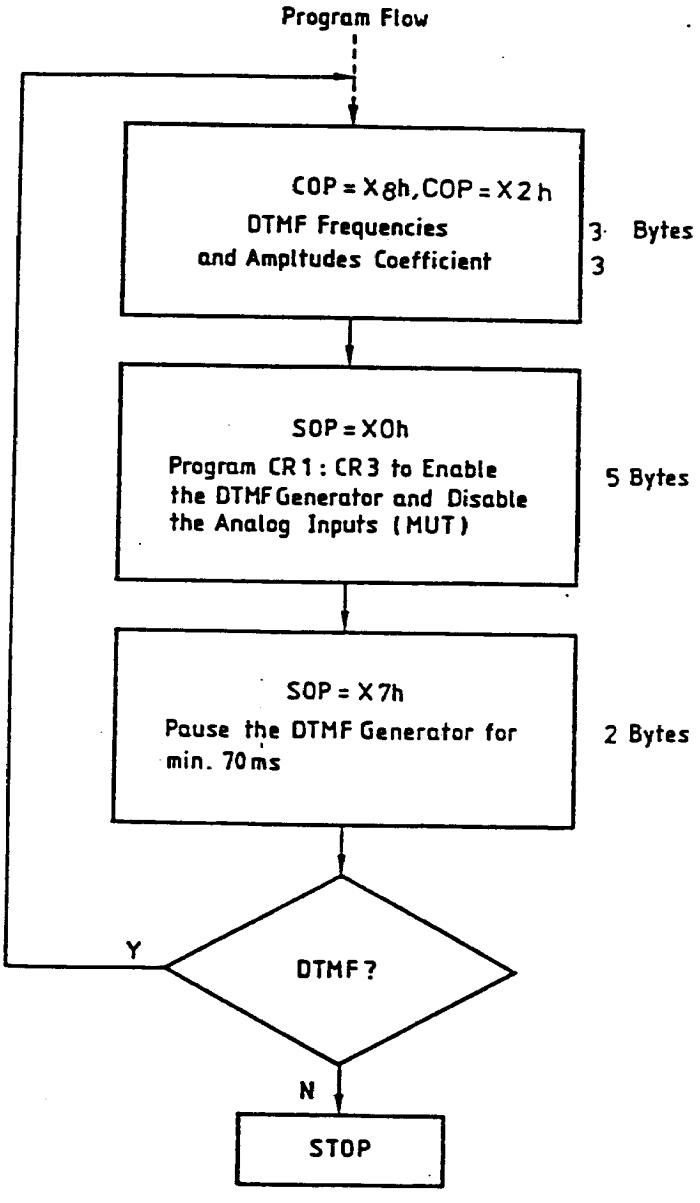
* : The deviations due to the inaccuracy of the incoming clock CK, when added to the nominal deviations tabulated above give th total absolute deviation from the CCITT recommended frequencies.

ex: To send the DTMF pair 770Hz + 1477Hz, the following COP sequence has to be generated by the µP

COP_E	+ C1	+ C2
h0E	hA8	h10

The DTMF signals of the high frequency group are programmed by default to generate a -2.2 dBmO PCM level for a 0 dB GX gain setting.

FIG 3.2.5 DTMF PROGRAMMING SEQUENCE



3.3 RECEIVE PATH SIGNAL PROCESSING

In the receive path the incoming PCM signal is expanded into a linear code according to the selected A or μ-LAW. If the linear mode is chosen, the PCM expander circuit is by-passed and a 16 bit linear word has to be provided to the processor.

A programmable sidetone gain stage Z adds a sidetone signal to the incoming voice signal. The sidetone gain can be programmed from -50 to -2.5 dB within a +/- 1dB tolerance range.(0dB is also possible). On reset the default Z gain value is -18dB.

The FR frequency correction filter is similar to the FX filter allowing an optimum adaptation to different type of loudspeakers and earpieces.

A low pass EWDF filter limits the signal bandwidth in the receive direction according to CCITT recommendations (see Fig. 3.2.1 and 3.2.2). The GR gain adjustment stage is digitally programmable from -45dB to +12dB within a 0.25dB tolerance range. Two bytes are coded in the CRAM to set GR to the desired value. On reset the initial GR setting is 0dB. A series of low pass interpolation filters increase the sampling frequency up to 128kHz. The last interpolator feeds the D/A converter.

3.3.1 TONE RING AND TONE GENERATOR

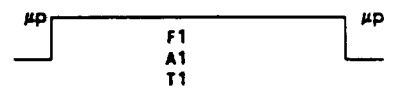
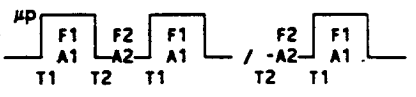
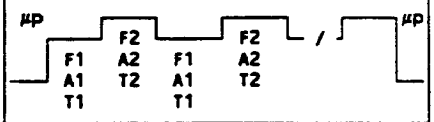
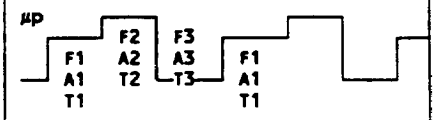
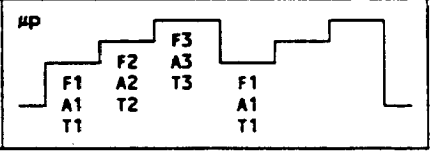
The ASP receive path contains two signal generators; a tone ring and a beat tone generator (TR & BT). Those generators can be used for tone alerting, call progress tones or other audible feedback tones. All generated tones can be provided at either the handset earpiece, the loudspeaker output or the piezo ringer output (SA & SB).

Distinctive alerting signals allowing for example the use of different multitone ringing patterns, are all programmable using the beat tone generator in conjunction with the tone ringer. In the case of a two or three tone ringing signal, the tone ring generator controls the outputed frequency pitch whilst the beat tone generator controls the repetition rate.

Examples of the complex pattern involving the repetition of multifrequency signals with different duty cycles are shown if Fig. 3.3.2. Tones can be superimposed on the incoming voice signal or can be outputed separately to the piezo ringer output. The tones can also be low passed or directly applied as a square wave to the D/A output. The tone generators can be programmed to specify frequencies, amplitudes and repetition rates through a COP command. Two bytes in the CRAM are necessary to set the frequency. An additional byte is necessary to set the amplitude and two bytes are required for the timing rate.

Five distinctive bits in configuration register 4 (CR4) control the ARCOFI tone generator. The tone generator TG and beat tone BT bits enable or disable the generators. Tone mode bit TM selects or deselects the mixing of voice and tones. Piezo mode bit PM select to which output the tone will go: piezo output (pins SA & SB) or D/A. Beat mode bit BM selects a two or a three tone ring signal pattern.

3.3.2 TONE PATTERNS EXAMPLES

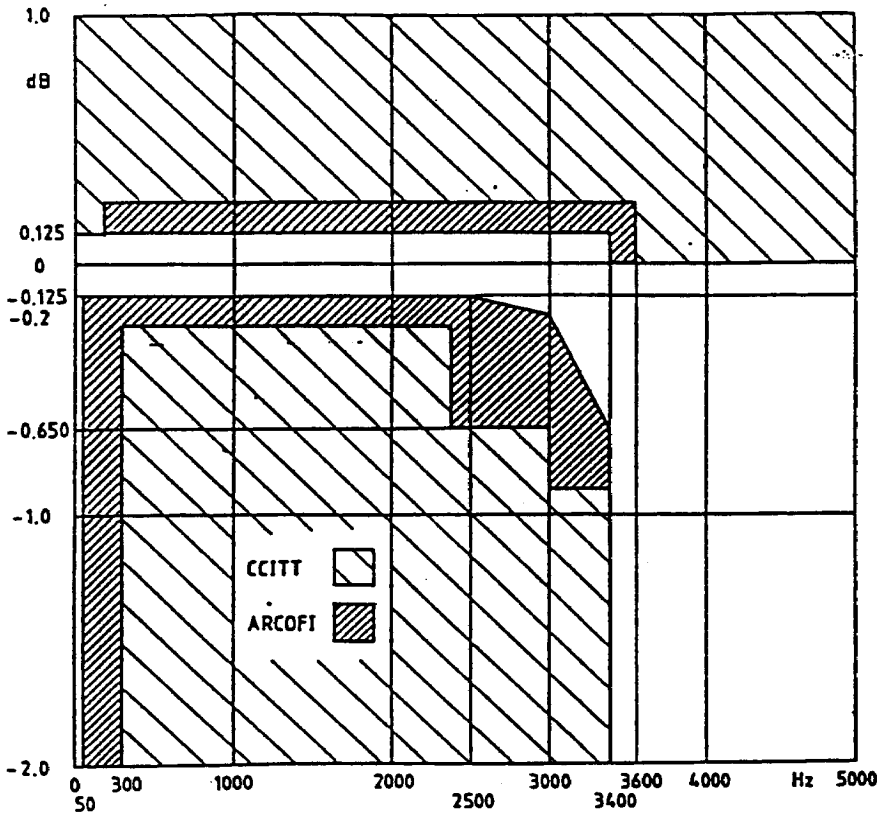
Name	CR1,CR2	Coefficient range	PATTERN
Constant single Tone	TG = 1 BT = 0 BM = 0 *)	F1: 6,5 to 3600Hz A1: -50 to 0 dB T1: 5ms to 16s	
Cycled single tone	TG = 1 BT = 1 BM = 0	F1:F2;6,5 to 3600Hz A1:A2;-50 to 0 dB T1:T2;5ms to 16s	
Cycled two tones without pauses	TG = 1 BT = 1 BM = 0	F1:F2;6.5 to 3600Hz A1:A2;-50 to 0 dB T1:T2;5ms to 16s	
Cycled two Tones with pauses	TG = 1 BT = 1 BM = 1	F1:F2:F3;6.5 to 3600Hz A1:A2:A3;-50 to 0 dB T1:T2:T3;5ms to 16s	
Cycled three Tones without pauses	TG = 1 BT = 1 BM = 1	F1:F2:F3;6.5 to 3600Hz A1:A2:A3;-50 to 0 dB T1:T2:T3;5ms to 16s	

F1 : first frequency coefficient
A1 : first amplitude coefficient
T1 : first Beat generator timing coefficient
x : don't care

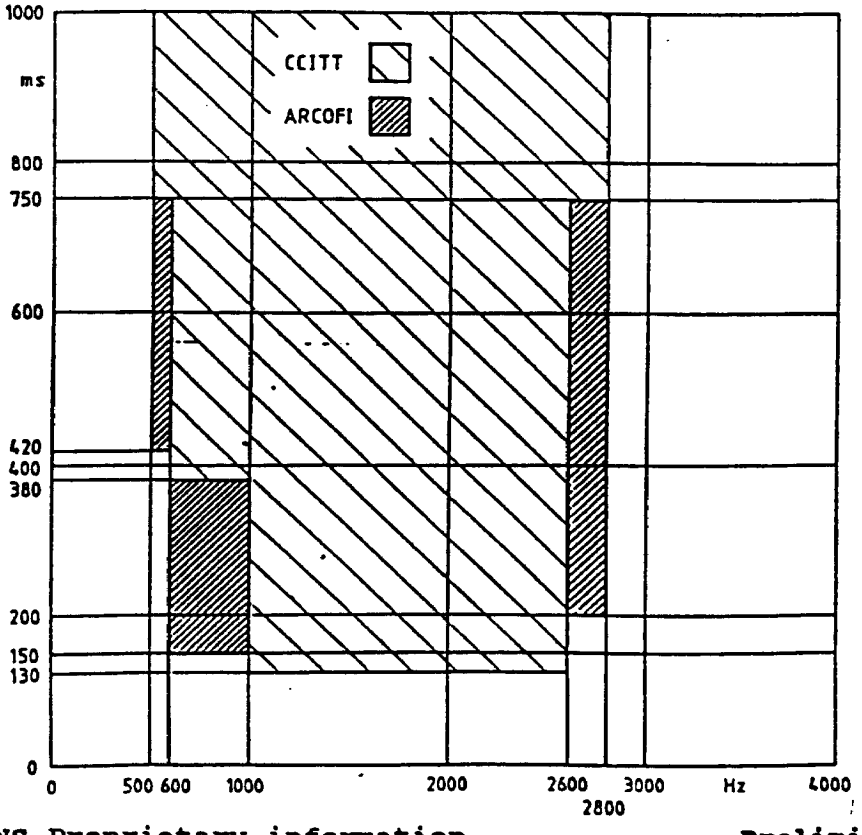
µp : microprocessor intervention through COP & SOP commands

*) : When BM=1 the selected coefficient set is F2,A2,T2

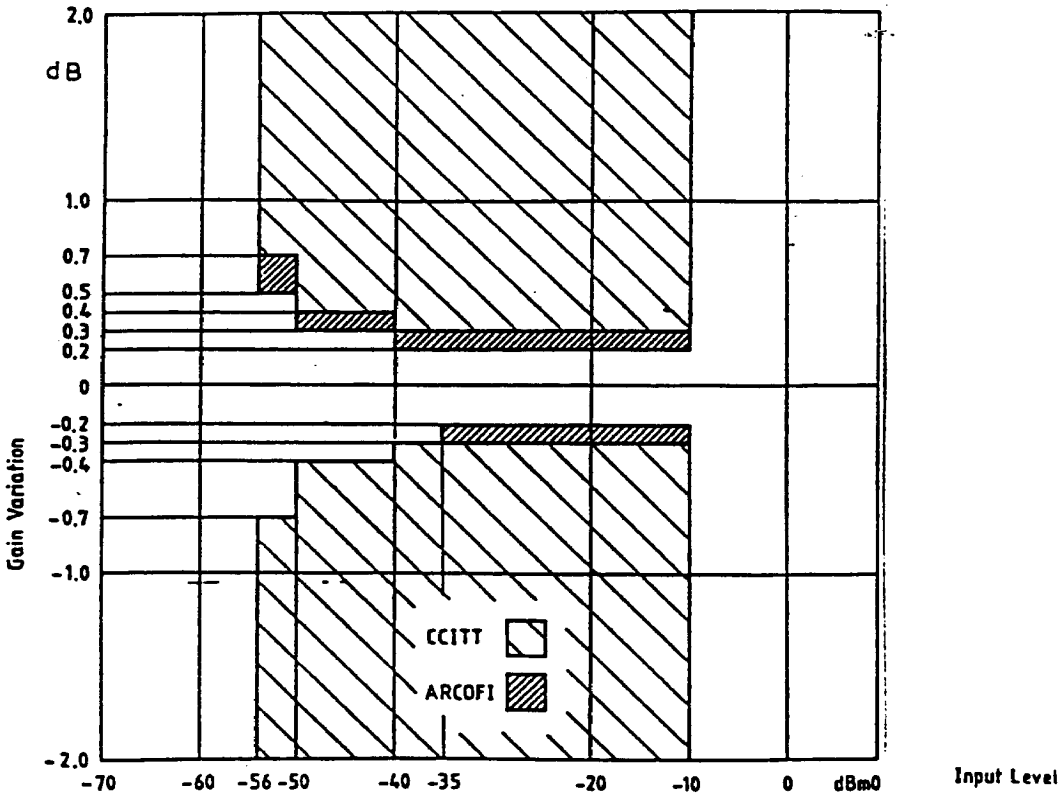
3.3.3 ATTENUATION DISTORTION IN RECEIVE DIRECTION



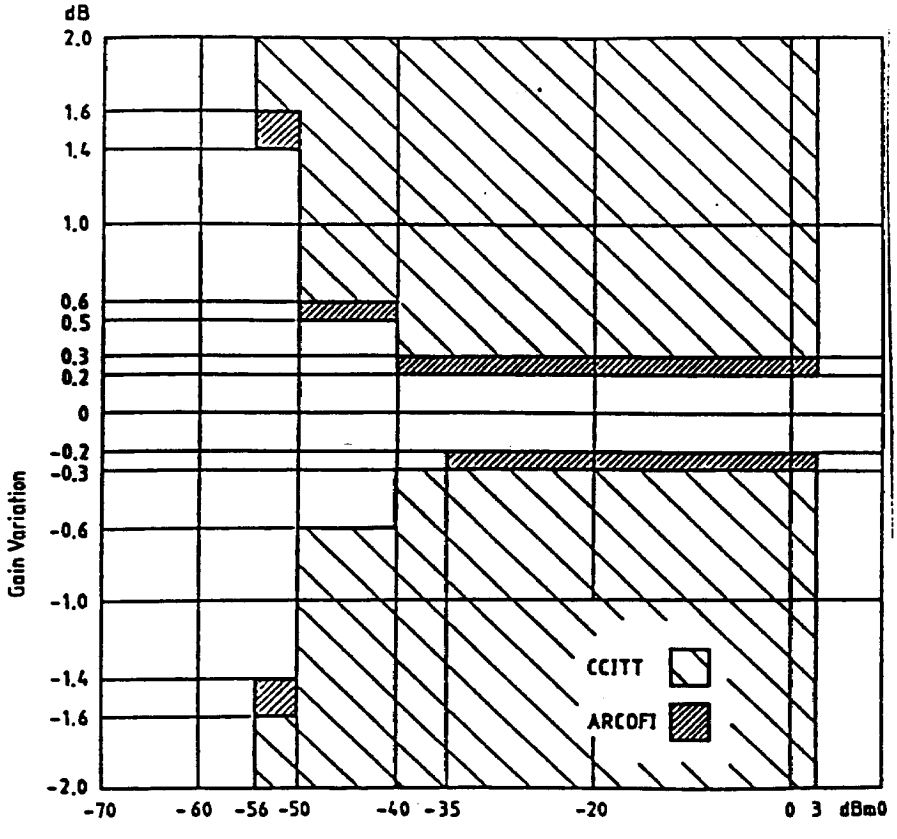
3.3.4 GROUP DELAY DISTORTION IN RECEIVE DIRECTION (ref 1500 Hz)



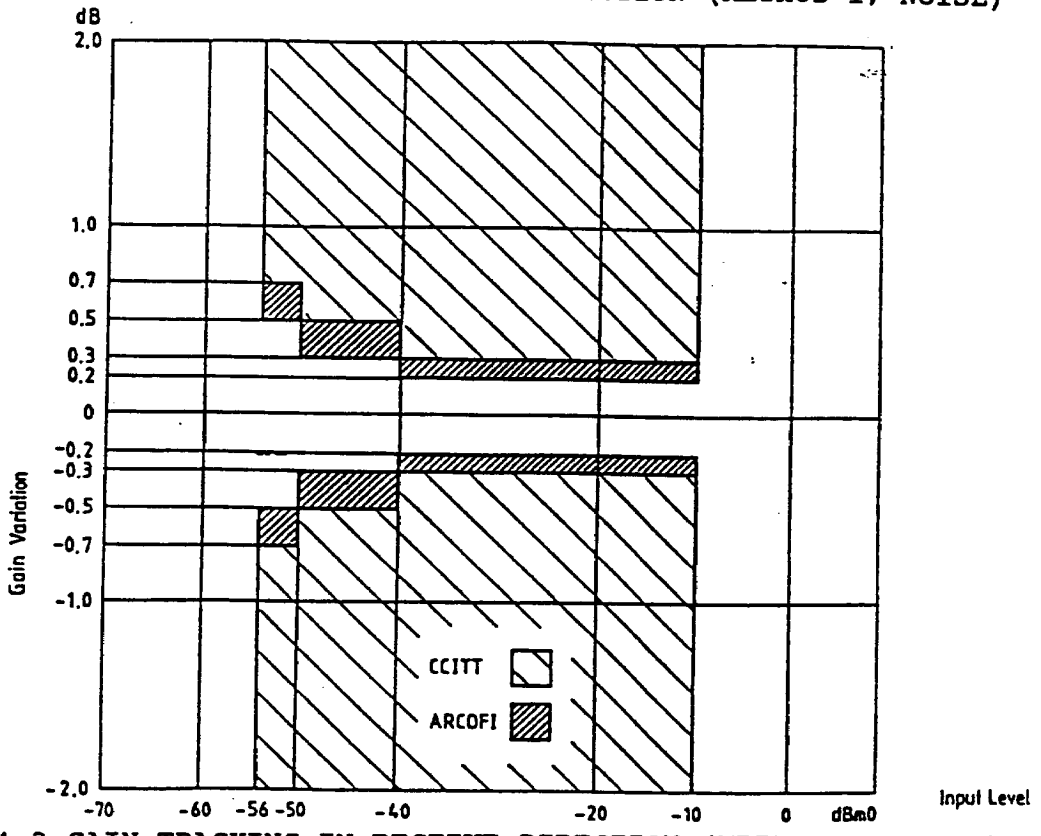
3.4 GAIN TRACKING IN TRANSMIT DIRECTION (METHOD 1; NOISE)



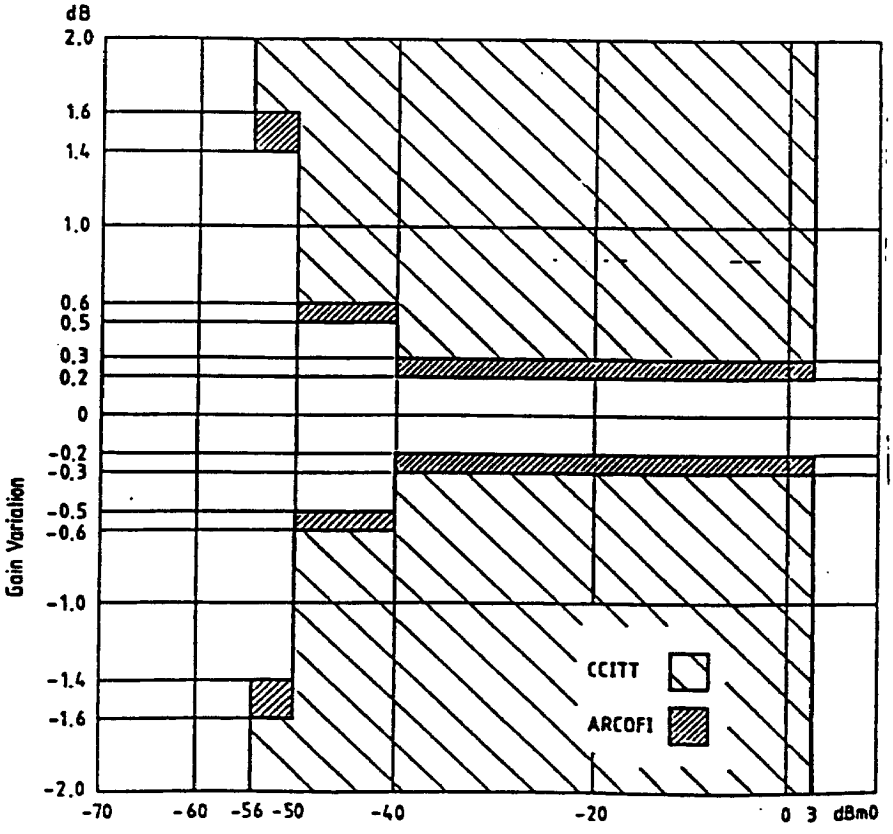
3.4.1 GAIN TRACKING IN TRANSMIT DIRECTION (METHOD 2; SINUS)



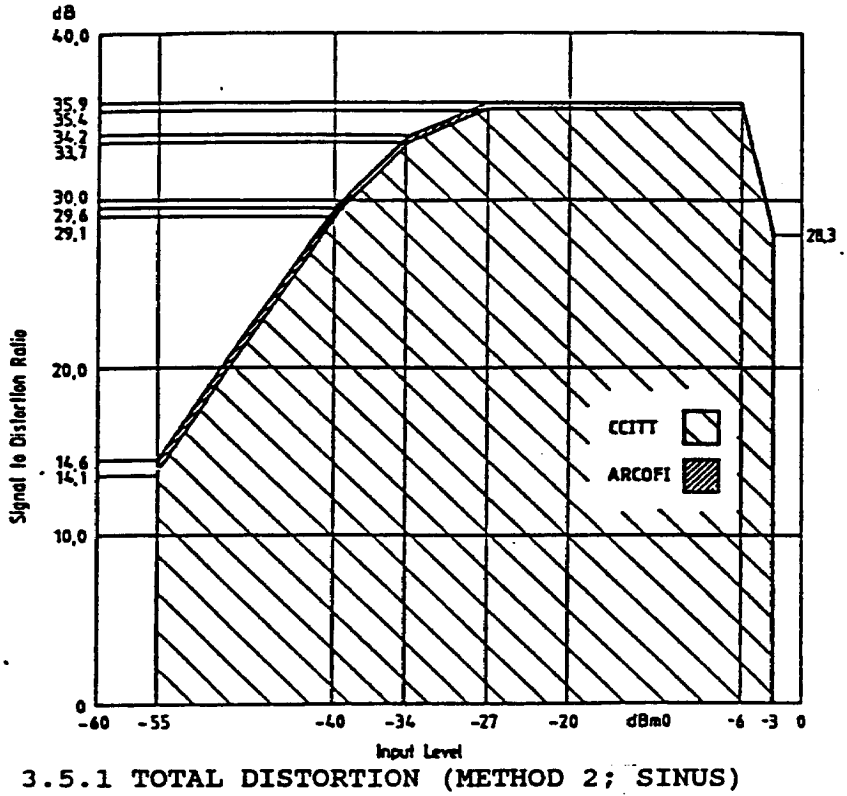
3.4.2 GAIN TRACKING IN RECEIVE DIRECTION (METHOD 1; NOISE)



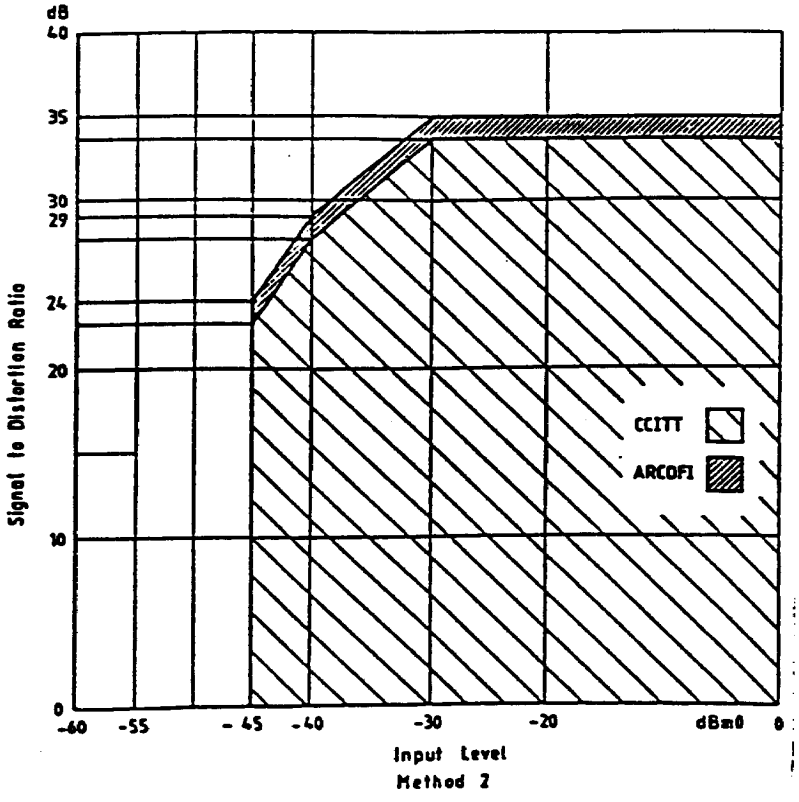
3.4.3 GAIN TRACKING IN RECEIVE DIRECTION (METHOD 2; SINUS)



3.5 TOTAL HARMONIC DISTORTION (METHOD 1; NOISE)



3.5.1 TOTAL DISTORTION (METHOD 2; SINUS)



4.0 ARCOFI DIGITAL INTERFACES (ADI)

The Arcofi Digital Interface section consists of a serial interface bus which can be configured to be compatible to the SLD or the IOM(TM) Rev2 standard and a set of four programmable I/O pins grouped as a Peripheral Control Interface (PCI).

4.1 IOM(TM) Rev2 interface

The IOM(TM) Rev2 interface consists of two data lines and two clock lines. DU: Data Upstream carries data from the ARCOFI to the layer 1 device and DD: Data Down stream carries data from the layer 1 device to the ARCOFI. An FSC frame synchronization clock is supplied to the ARCOFI as well as a DCL 1.536 MHz data clock for bit clocking.

Selecting between the IOM(TM) Rev2 or the SLD interfacing mode is performed by strapping pin SP1 & SP2 according to the pin strapping function table 4.3.2

The ARCOFI implements all IOM(TM) Rev2 terminal functions spelled out in the IOM(TM) Rev2 interface specification, where a more precise description of IOM(TM) Rev2 can be found.

4.2 SLD interface (see FIG 4.2.1)

The SLD Serial interface consists of a bidirectional data line **SIP** a synchronization clock input **CK** and a data direction input **FSC**. Data bits are loaded or read out of the serial interface pin SIP under control of a direction signal FSC. Bits are clocked in or clocked out on the rising edge of the slave clock pin CK (512kHz). FSC and CK inputs must be phase locked.

An SLD frame lasts 125 µs and consists of 32 bits transferred to the ARCOFI (FSC high) followed by 32 bits transferred from the ARCOFI to the SLD bus (FSC low).

The SLD interface thus provides a full duplex 256kb/s communication capacity. This capacity is subdivided in two 64kb/s voice/data channels reserved for the ISDN B1 and B2 channels. The remaining bandwidth is used by a feature control channel (64kb/s) and a signalling channel (64kb/s). Bytes in all channels are serialized MSB first.

A command received over the SLD can cause a response over the SLD within the same frame. This leaves the ARCOFI 31.25 µs to interpret the command and generate the appropriate answer in the following half frame TX command channel.

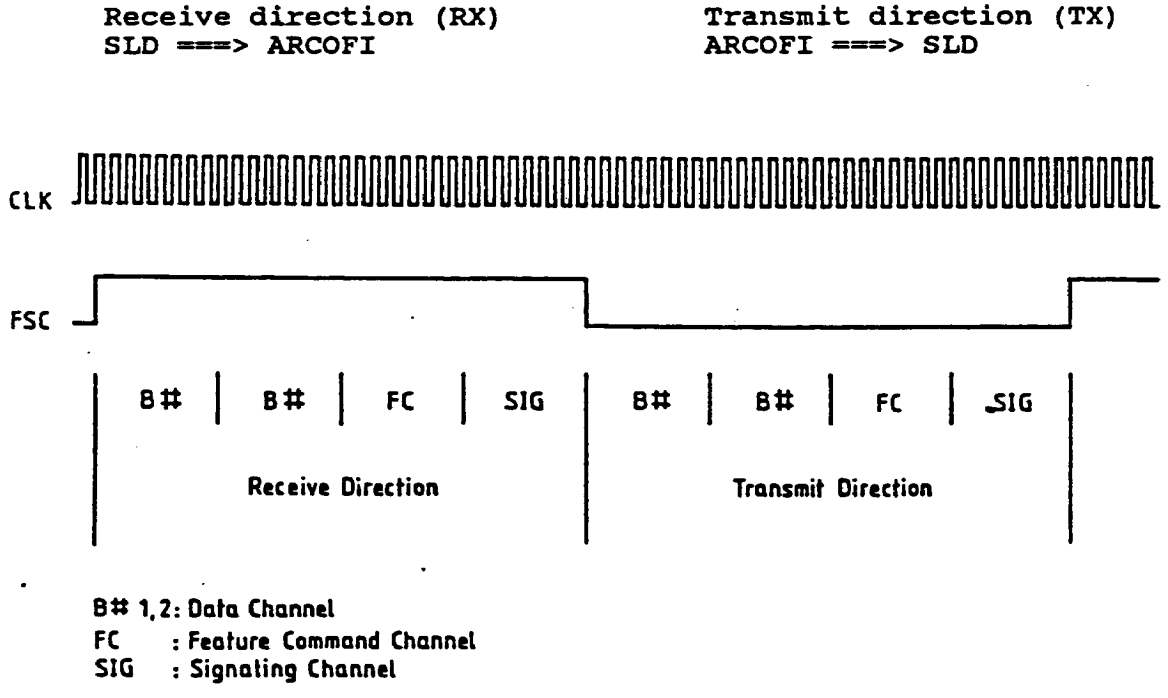
All ARCOFI internal registers are accessible via the SLD bus in the time slot allocated to the command channel. The first byte transferred in the command channel specifies the type of operation and the number of bytes allocated to the transfer set-up according to the coding table described in the section "Command Register". In a multiple byte transfer the ARCOFI address register points to the first location implied in the command register bit field CB0-CB3. Following bytes transfer in successively higher order locations.

When in power down (PU=0 ;CMDR), the command channel remains active in both transmit and receive direction providing that the address bit (AD ;CMDR) matches the address strapped on SP1,SP2(see supplementary functions). In power down however both data channels are disabled; SIP being tristated during data channel transmit time slots.

If the linear mode is selected (LIO 2 = 1,0 ;CR3) a full linear 16 bits word is transmitted or received in the data channels B1 & B2.

If mixed mode is selected (LIO 1 = 0,1 ;CR3) a full linear 16 bits word is transmitted in the TX-FC & TX-SIG channels. This option is available only if ELS = 0 in CR2

FIG 4.2.1 SLD Bus



B# 1,2: Data Channel
FC : Feature Command Channel
SIG : Signaling Channel

4.2.1 SLD BUS CONTENTION RESOLUTION

When connecting more than one device to the SLD bus, the access to the Transmit Bearer, Feature control and signalling channels has to be managed so as to avoid contention on the SIP line. Each individual channel will be considered separately and the proper configuration bit set-up when accessing a particular channel will be described.

4.2.2 BEARER/DATA CHANNEL CONTENTION RESOLUTION

Contention may arise in the Bearer channel TX-B1 and TX-B2 if two devices connected to the SIP line try to access these channel simultaneously.

When powered down (PU=0 ; CMDR) both data channels are ignored (TX-B1 & TX-B2 tristated). When activated (PU=1 in CMDR) only one channel is active according to the bit setting in the CMDR (RCS = 1; RX & TX-B2 active. RCS = 0; RX & TX-B1 active), the other Bearer/Data channel is tristated if CR2 bit AM=0, otherwise NOP's are transmitted in the non selected channel.

If mixed mode is selected (LIO = 0,1 in CR3) both channels are activated, thus no access is allowed from an other SLD connected device. It is up to the user, after a power on reset to properly select the use of the bearer/data channels so as to avoid contention.

When two ARCOFI's are connected to the SLD bus, each using a different bearer channel, it is possible to swap channels using the following procedure:

a) command ARCOFI#1 to power down and SWAP bearer channels
b) command ARCOFI#2 to SWAP bearer channels
c) command ARCOFI#1 to power up

The ARCOFI#1 lose two received/transmit word when following this procedure.

4.2.3 FEATURE CONTROL CHANNEL CONTENTION RESOLUTION

Contention in the Feature control (FC) channel when issuing a SOP or COP read command:

If the received SOP or COP command bit AD matches the strapped address on Pin SP1 and SP2, the SIP buffer is activated during the following TX-FX time slots until the entire read sequence has been executed, the SIP buffer return to tristate thereafter if AM=0, otherwise NOP's are transmitted.

4.2.4 SIGNALLING CHANNEL CONTENTION RESOLUTION

When two or more devices share the TX-SIG channel, care must be taken to avoid collision. When the ELS & AM bits are set to one in CR2, the SA - SD pins which are not programmed as TX-SIG inputs are tristated. Depending on the programming of AM & EL, the TX-SIG bits which are not defined as inputs are transmitted as 0 or are tristated (see 4.3.6 signalling channel bit allocation table).

4.3 ARCOFI PERIPHERAL CONTROL INTERFACE (PCI)

The ARCOFI Peripheral Control Interface (PCI) consists of 6 pins; 4 pins SA to SD are used as a peripheral control port and can be programmed individually as inputs or outputs.

The remaining two pins SP1 and SP2 are used to address the device and to implement supplementary functions.

4.3.1 PCI PINOUT DESCRIPTION

The ARCOFI communicates with the terminal equipment microcontroller through either the SLD or the IOM(TM) Rev2 bus.

In the SLD interfacing mode all internal registers including the coefficient RAM are solely accessible using the command register as an address pointer. The signalling channel is transparent to the ARCOFI and is routed to the four SA-SD pins.
This allows SA-SD to be used as peripheral control interface lines.

Pins SA-SD can be configured individually as inputs or outputs. A quarter of the total available signalling channel bandwidth is routed this way to the PCI port, the remaining signalling channel capacity can be made available through the use of an expansion option.

4.3.2 SUPPLEMENTARY FUNCTIONS TABLE

Supplementary functions are accessed by strapping pins SP1 and SP2 according to the following table:

Pin SP1	Pin SP2	Chip Address	PLL/ EXT	Mode sel SLD/IOM	Description
-1	0	X			
-1	-1	X	EXT	SLD fast	TEST mode 1
-1	1	X	PLL	SLD fast	TEST mode 2
0	1	AD=0	PLL	SLD slow	PLL circ. enabled the SLD transfer rate is CK. *1)
1	1	AD=1	PLL	SLD slow	
0	0	AD=0	PLL	IOM	PLL circuit is enabled,the IOM rate is 1.536 MHz *2)
1	0	AD=1	PLL	IOM2	
0	-1	AD=0	EXT	SLD fast	PLL circuit is by passed, SLD rate is the internal master clock CK
1	-1	AD=1	EXT	SLD fast	

-1 = -5 Volt (VSS) ; 1 = 5 Volts (VDD) ; 0 = 0 Volt(GNDD)

*1) When powered down (PU=0 in CMDR) both data channel are also ignored (TX-B1 & B2 high Z). Thus the SLD bus is free for external device access

*2) Release 1A of the ARCOFI do not implement the IOM(TM) Rev2 mode but instead the PLL circuit is by-passed with an SLD transfer rate of CK/8

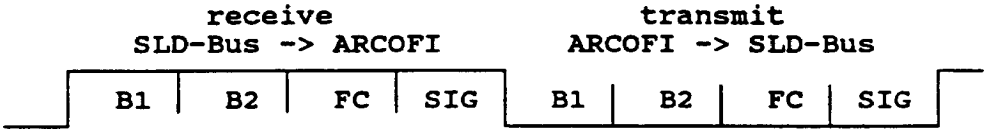
4.3.3 SLD TRANSFER RATE MODE

The ARCOFI operates either from an on chip generated 4.096MHz master clock derived by an internal PLL circuit supplied from the 512 kHz slave clock CK (PLL on), or the PLL circuit is by-passed and the internal master clock rate equals the externally supplied clock on pin CK (EXT).

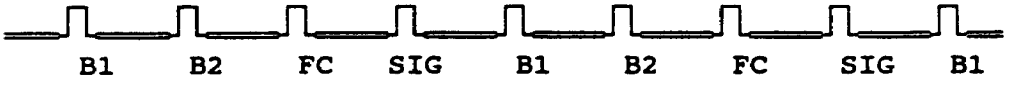
Two data transfer modes are possible on the SLD-Bus: a "slow mode" (512 kHz slave clock or frequency of the external CK when the PLL is on) and a "fast mode" (internal master clock rate or CK when the PLL is by-passed).

The selection of the supplied clock and the SLD clock rate is made via Pins SP1, SP2 as listed in the preceding supplementary function table.

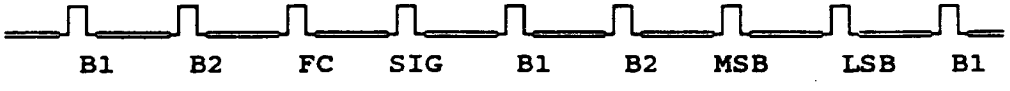
In "fast mode" 8 or 16 bits are transferred depending on the programmed I/O mode (CR3: Bits LIO).



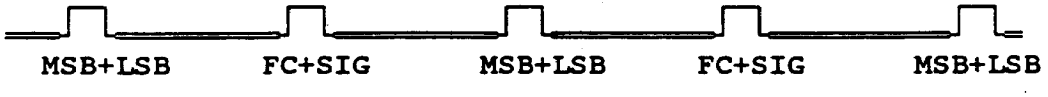
a) LIO bits 0 0; normal I/O mode



b) LIO bits 0 1; mixed I/O mode



c) LIO bits 1 0; linear I/O mode



 ... high Z

 ... Transfer 8 bit via SLD-Bus at 4MHz

 ... Transfer 16 bit via SLD-Bus at 4MHz

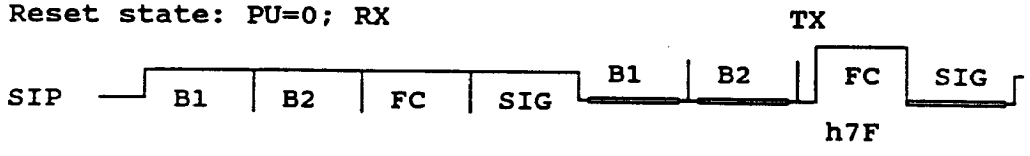
B1,B2 ... 8 bit PCM data
MSB+LSB ... 16 bit linear data
FC ... control byte
S ... signalling byte

*) during the processing of a COP or SOP read instruction the ARCOFI sends feature control and signalling Bytes. During COP or SOP write,NOP's are sended back.

4.3.4 ARCOFI RESET FLAG

A reset flag "R" monitors the reset pin of the ARCOFI. When a reset is asserted the R flag is cleared. This is indicated by bit 7 being set to 0 during TX-FX NOP time slots (7F hex is transmitted instead of the normal NOP's FF hex). Flag R can be set to one by performing a CR4 to CR1 SOP_0 write operation. All configuration registers are cleared after a reset has been asserted and need to be reconfigured anyway.

So as to read out the status of the R flag the TX-FX channel has to be activated as described in section 4.2.3, feature control channel contention resolution.



4.3.5 EXPANSION OPTION

To fully use the signalling channel bandwidth capacity an expansion option has been devised. If the ELS bit in the configuration register CR2 has been set to 1 the expansion option is considered to be connected. In the receive direction, the PCI pins SA-SD which have been programmed as outputs receive data from the corresponding bits in the RX-SIG channel. Remaining bits can thus be allocated to a second device connected to the SLD bus. In the transmit direction, the PCI pins which have been connected as inputs transfer data in the corresponding bits of the TX-SIG channel. During the remaining bits transfer SIP is tristated allowing a second device on the SLD bus to transfer PCI data. The ELS option is independent from the address bit setting (AD,bit 7) in CMDR. The user must consequentialy program the PCI pins to avoid contention on the SLD bus.

4.3.6 SIGNALLING CHANNEL BIT ALLOCATION TABLE

RECEIVE-SIG 7 6 5 4 3 2 1 0	TRANSMIT-SIG 7 6 5 4 3 2 1 0	CONFIGURATION AM	ELS	CASE
X X X X X X X X	S S S S D C B A 0 0 0 0	1	0	one chip
X X X X X X X X	S S S S D C B A Z Z Z Z	1	1	PCI pins as INPUTS
S S S S D C B A X X X X	0 0 0 0 0 0 0 0	1	0	one chip
S S S S D C B A X X X X	Z Z Z Z Z Z Z Z	1	1	PCI pins as OUTPUTS
1#X X X X X X X X	S S S S D C B A Z Z Z Z	0	1	two chips
2#X X X X X X X X	S S S S Z Z Z Z D C B A	0	1	PCI pins as INPUTS
S S S 1#D C B A X X X X	0 0 0 0 Z Z Z Z	0	0	two chips
2#X X X X D C B A	Z Z Z Z 0 0 0 0	0	0	PCI pins as OUTPUTS
S S 1#X X B A X X X X	S S D C 0 0 Z Z Z Z	0	0	two chips
S S 2#X X X X D C X X	Z Z Z Z 0 0 S S B A	0	0	PCI pins IN & OUT

X: don't care
Z: tri-state

ARCOFI EXPANSION OPTION USE EXAMPLE

ARCOFI #1 PCI pins SA & SB are configured as outputs the remaining pins are inputs
ARCOFI #2 PCI pins SC & SD are configured as outputs the remaining pins are inputs

According to this selection a quarter of the PCI channel capacity is directed to ARCOFI #1, an other quarter is directed to ARCOFI #2. The following timing diagram indicates where the allocated bits are transferred.

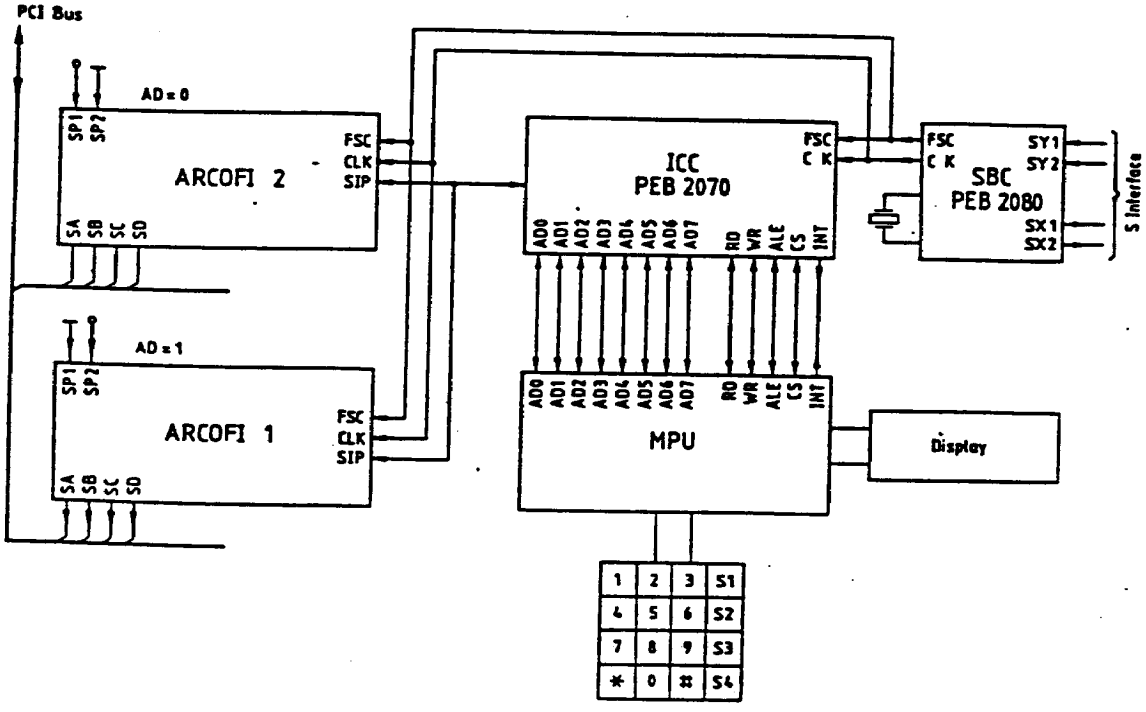
The following bits are defined in the CMDR and CR registers

ARCOFI #1 : AD=0; AM=0; RCS=1; ELS=0; TR=0; (EFC=1)
ARCOFI #2 : AD=1; AM=0; RCS=0; ELS=0; TR=0; (EFC=0)

Time slot	t0			
Transfer direction	RX ARCOFI#1	RX ARCOFI#2	TX ARCOFI#1	TX ARCOFI#2
CH - B1	X	B1/7-B1/0	SIP high Z	B1/7-B1/0
CH - B2	B2/7-B2/0	X	B2/7-B2/0	SIP high Z
FC - CH	AD=0 CMB7-0	X	AD=0 CMB7-0	SIP high Z
SIG - CH	rest is X	rest is X	rest SIP high Z	rest SIP high Z

X: don't care

FIG 4.3.7 SLD EXPANSION OPTION



4.4 ARCOFI INTERNAL REGISTER DESCRIPTION

The following describes the various ARCOFI registers and coefficient RAM locations accessible from the terminal equipment microcontroller via the SLD bus.

A summary of the 9 registers located in the ADI block is presented below followed by a detailed description of the register content.

Serial interface port register (SIPR)

	7	6	5	4	3	2	1	0
SIPR	SIP7	SIP6	SIP5	SIP4	SIP3	SIP2	SIP1	SIP0

Command register (CMDR)

	7	6	5	4	3	2	1	0
CMDR	AD	R/W	PU	RCS	CMB3	CMB2	CMB1	CMB0

Configuration register 1 (CR1)

	7	6	5	4	3	2	1	0
CR1	GR	GZ	FX	FR	GX	TMB2	TMB1	TMB0

Configuration register 2 (CR2)

	7	6	5	4	3	2	1	0
CR2	SD	SC	SB	SA	ELS	AM	TR	EFC

Configuration register 3 (CR3)

	7	6	5	4	3	2	1	0
CR3	AGX			AFEC			LIO	

Configuration register 4 (CR4)

	7	6	5	4	3	2	1	0
CR4	DHF	DTMF	TG	BT	TM	BM	PM	A/μ

CONT'D

Peripheral control interface register(PCIR)

	7	6	5	4	3	2	1	0
PCIR	X				PCB3	PCB2	PCB1	PCB0

X:don't care

Pulse code modulation register 1 (PCMR1)

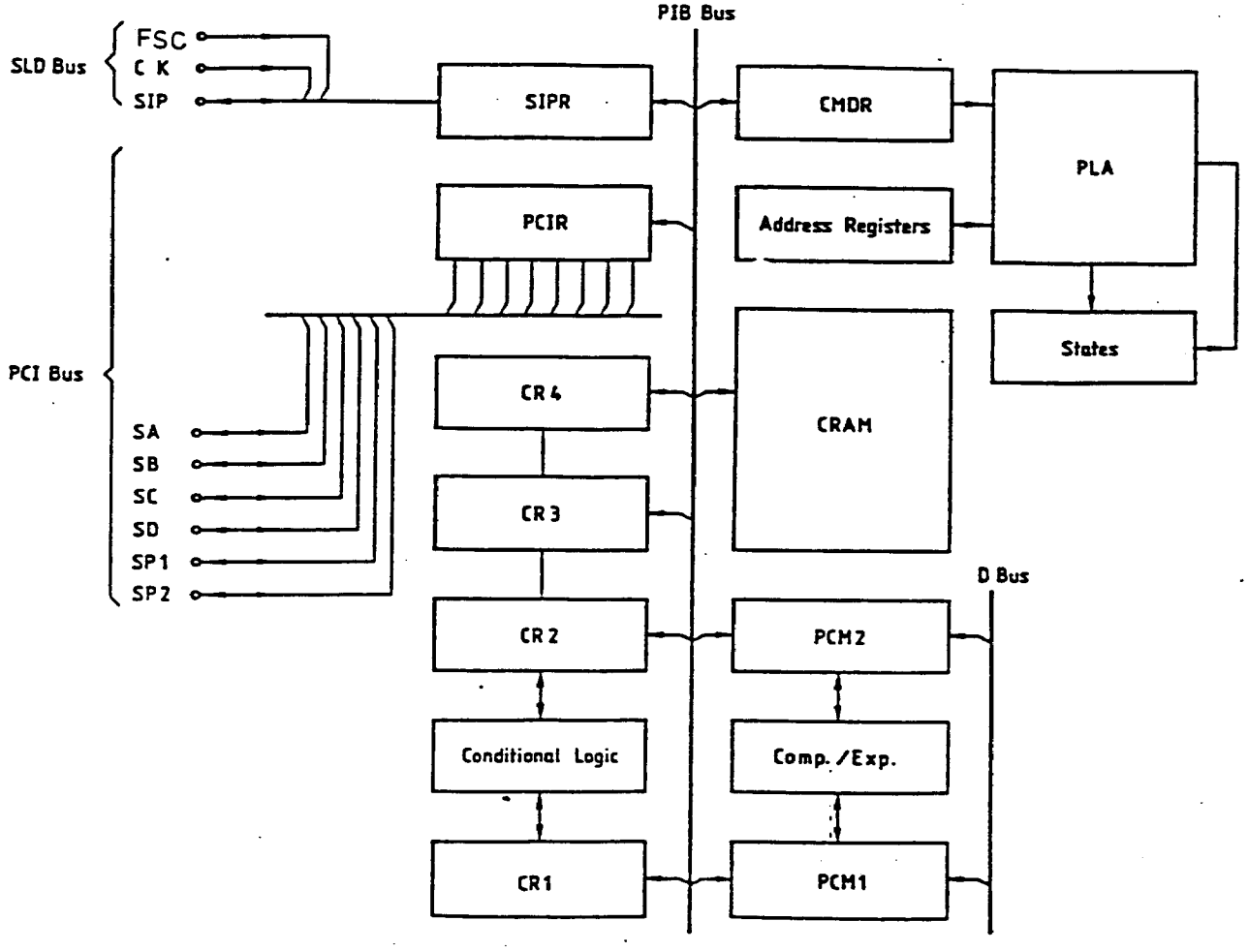
	7	6	5	4	3	2	1	0
PCMR1	PLB7	PLB6	PLB5	PLB4	PLB3	PLB2	PLB1	PLB0

Pulse code modulation register 2 (PCMR2)

	7	6	5	4	3	2	1	0
PCMR2	PHB7	PHB6	PHB5	PHB4	PHB3	PHB2	PHB1	PHB0

X: don't care

FIG 4.4 ARCOFI ADI REGISTERS



4.4.1 COMMAND REGISTER (CMDR)

	Logical 1	Logical 0
BIT 7	AD=1 ; if bit AD match the address convention strapped on SP1,SP2; pin SIP is active as output during SLD-TX slots	AD=0 ; if address bit is not consistent with the logical level strapped on SP1/2; SIP tristated during SLD transmit time slots
BIT 6	R/W=1 ; reading from CMDR,CR1,CR2,CR3,CR4 or CRAM	R/W=0 ; writing to CMDR,CR1,CR2,CR3,CR4 or CRAM
BIT 5	PU=1 ; The ARCOFI is in a normal operating mode (powered up)	PU=0 ; The ARCOFI is placed in stand by (powered down). All register contents are saved
BIT 4	RCS=1 ; receive and transmit in CH-B2 (see SLD bus description).	RCS=0 ; receive and transmit in CH-B1.

COMMAND REGISTER (CMDR) CONT'D

A full sequence consist of a command byte followed by <..>n byte coefficients.

BIT 3 2 1 0	CMD NAME	STATUS MODE	CMD SEQUENCE LENGTH	CMD SEQUENCE DESCRIPTION	;COMMENTS
0 0 0 0	SOP_0	R/W	5	<CR4><CR3><CR2><CR1>	;Reset F flag
0 0 0 1	COP_1	R/W	5	<t1><t1><f1><f1>	;Beat tone time span T1 & ;tone generation frequency F1
0 0 1 0	COP_2	R/W	3	<gx1><gx2>	;GX gain
0 0 1 1	COP_3	R/W	5	<t2><t2><f2><f2>	;Beat tone time span T2 & ;tone generation frequency F2
0 1 0 0	SOP_4	R/W	2	<CR1>	;Configuration register 1
0 1 0 1	SOP_5	R/W	2	<CR2>	;Configuration register 2
0 1 1 0	SOP_6	R/W	2	<CR3>	;Configuration register 3
0 1 1 1	SOP_7	R/W	2	<CR4>	;Configuration register 4
1 0 0 0	COP_8	R/W	3	<dtmf_high><dtmf_low>	;DTMF frequencies
1 0 0 1	COP_9	R/W	5	<gz><a3><a2><a1>	;GZ gain & tone generator ;amplitudes A1,A2,A3
1 0 1 0	COP_A	R/W	9	<fx1><fx2><fx3><fx4> <fx5><fx6><fx7><fx8>	;FX frequency correction coef- ;ficient set 1
1 0 1 1	COP_B	R/W	3	<gr1><gr2>	;GR gain
1 1 0 0	COP_C	R/W	9	<fr1><fr2><fr3><fr4> <fr5><fr6><fr7><fr8>	;FR frequency correction coef- ;ficient set 1
1 1 0 1	COP_D	R/W	5	<fr9><fr10><fx9><fx10>	;FX & FR coefficient set 2
1 1 1 0	COP_E	R/W	5	<t3><t3><f3><f3>	;Beat tone time span T3 & ;tone generation frequency F2
1 1 1 1	NOP	R		<hFF>	;No operation, CMDR ;bits 7,6,5,4 are masked
		W			;No operation, CMDR ;bits 7,6,5,4 can be written

W: ;write
R: ;read
<..> ;mandatory byte coefficient sequence

BITS	7	6	5	4	3	2	1	0
	AD	R/W	PU	RCS	CMB3	CMB2	CMB1	CMB0

Initial value on RESET : 0Fh (NOP)

4.4.2 CONFIGURATION REGISTER 1 (CR1)

	Logical 1	logical 0
BIT 7	GR=1 ; GR gain loaded from CRAM	GR=0 ; GR gain set to 0dB
BIT 6	GZ=1 ; Z gain loaded from CRAM	GZ=0 ; Z gain set to -18 dB
BIT 5	FX=1 ; X filter loaded from CRAM	FX=0 ; X filter set to 0dB flat
BIT 4	FR=1 ; R filter loaded from CRAM	FR=0 ; R filter set to 0dB flat
BIT 3	GX=1 ; GX gain loaded from CRAM	GX=0 ; GX gain set to 0dB

BIT 2 1 0	Test mode	Configuration description
0 0 0	NOT	No test mode
0 0 1	ALS	Analog loop back via converter registers.
0 1 0	ALM	The MIC/Xin input loops back to HON & HOP. (Aho amplifier) the FHM input loops back to analog MUX. FHM input loops back to LSN & LSP. (Als amplifier)
2 1 1	BYP	By-pass: the analog front end is by-passed. FHM serves as a direct single ended input to the A/D converter while HOP outputs the single ended signal generated by the D/A converter
1 0 0	IDR	Data RAM initialisation, reset all data RAM locations to hex 00
1 0 1	DLS	Digital loop back via converter registers.
1 1 0	DLM	The D/A output is looped back to the A/D input via the analog I/O mux
1 1 1	DLP	Digital loop back via PCM registers

BITS

7	6	5	4	3	2	1	0
GR	GZ	FX	FR	GX	TMB2	TMB1	TMB0

Initial value on RESET : 00h

4.4.3 CONFIGURATION REGISTER 2 (CR2)

	Logical 1	Logical 0
BIT 7	SD=1 ;SD pin programmed as input	SD=0 ;SD pin programmed as output
BIT 6	SC=1 ;SC pin programmed as input	SC=0 ;SC pin programmed as output
BIT 5	SB=1 ;SB pin programmed as input	SB=0 ;SB pin programmed as output
BIT 4	SA=1 ;SA pin programmed as input	SA=0 ;SA pin programmed as output
BIT 3	ELS=1 ;PCI pins SA-SD which are not programmed as TX-SIG transmit inputs tristate SIP in TX direction	ELS=0 ;pins SA-SD which are not TX-SIG inputs are sending zeros.
BIT 2	AM=1 ;only device one is connected to the SLD bus, send NOP's during TX-FC	AM=0 ;two devices are connected to the SLD bus, tristate SIP during TX-FC
BIT 1	TR=1 ;Three party conferencing enabled CH-B1 is added to CH-B2 in the RX direction	TR=0 ;Three party conferencing disabled
BIT 0	EFC=1; Enable feature control. TX-FC channel is enabled	EFC=0; TX-FC channel is disabled (high Z)

BITS	7	6	5	4	3	2	1	0
	SD	SC	SB	SA	ELS	AM	TR	EFC

Initial value on RESET: F9h

4.4.4 CONFIGURATION REGISTER 3 (CR3)

	Logical 1		Logical 0
BIT 7 6 5	Analog gain adjustment transmit for the MIC input. Gain factor tolerance range +/- 0.5 dB		
0 0 0	52.0 dB default on RESET	0 1 1	34,0 dB
0 0 1	46.0 dB	1 0 0	28.0 dB
0 1 0	40 dB	1 0 1	22.0 dB
1 1 1	X input enabled with a 15.1 dB amplification factor MIC input disabled	1 1 0	17.0 dB

BIT 4 3 2 Operating mode — Configuration description Analog Front End Control (AFEC)

code	state	MIC/Xin	FHM	Hout	LS out	comments
0 0 0	POR	off	off	off	off	power on reset
0 0 1	RDY	on	off	on	off	ready
0 1 0	LH1	off	off	off	on	loud hearing 1
0 1 1	LH2	on	off	off	on	loud hearing 2
1 0 0	LH3	on	off	on	on	loud hearing 3
1 0 1	HFS	off	on	off	on	hands free
1 1 0	MUT	off	off	on	off	mute
1 1 1	RES	X	X	X	X	reserved

X: don't care

BIT 1 0 — Operating mode — Linear Input/Output (LIO)

0 0	LIO 0 Normal I/O mode	B#1 B#2 FC SIG B#1 B#2 FC SIG
0 1	LIO 1 ;ELS = 0 Mixed I/O mode	B#1 B#2 FC SIG B#1 B#2 MSB LSB
1 0	LIO 2 Linear I/O mode	MSB LSB FC SIG MSB LSB FC SIG
1 1	LIO 3 reserved	

BITS

7	6	5	4	3	2	1	0
AGX			AFEC			LIO	

Initial value on RESET: 00h

4.4.5 CONFIGURATION REGISTER 4 (CR4)

	Logical 1	Logical 0
BIT 7	DHF=1 ; digital high pass in TX direction enabled	DHF=0 ; digital high pass in TX disabled
BIT 6	DTMF=1 ; DTMF generator enabled	DTMF=0 ; DTMF generator disabled
BIT 5	TG=1 ; tone ring enabled	TG=0 ; tone ring disabled
BIT 4	BT=1 ; Beat tone generator enabled	BT=0 ; Beat tone generator disabled
BIT 3	TM=1 ;Tone mode bit set, incomming voice is activated	TM=0 ; incoming voice is blocked
BIT 2	BM=1 ;Beat mode. 3 tone ring activated when BT generator enabled	BM=0 ; 2 Tone ring activated when BT generator enabled
BIT 1	PM=1 ;Piezo mode bit set, tone generator is outputed To the piezo ring pins SA & SB	PM=0 ; The tone generator is directed to the loudspeaker (D/A out)
BIT 0	A/μ=1; μ law enabled	A/μ=0; A law enabled

BITS	7	6	5	4	3	2	1	0
	DHF	DTMF	TG	BT	TM	BM	PM	A/μ

X: don't care

Initial value on RESET: 00h

4.5 ARCOFI PROGRAMMING VIA THE SLD BUS

Time slot	t2		t1		t2		t3		t4		t5	
Transfer direction	RX	TX	RX	TX	RX	TX	RX	TX	RX	TX	RX	TX
CH - B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1	B1
CH - B2	X	Z	X	Z	X	Z	X	Z	X	Z	X	Z
FC - CH	SOP	NOP	CR4	NOP	CR3	NOP	CR2	NOP	CR1	NOP	NOP SOP COP	
SIG - CH	SIG	SIG	SIG	SIG	SIG	SIG	SIG	SIG	SIG	SIG	SIG	SIG

X: don't care
Z: high impedance

4.5.1 ARCOFI CONTROL BYTE SEQUENCES IN THE FC TIME SLOT

RX:= Receive direction TX:= Transmit direction
X:= 1,2,3 or 4
FC:= NOP- or COP- or SOP-Command bytes in TX direction

DIR 1 0	NORMAL MODE	SOP WRITE		SOP READ			COP WRITE	COP READ
RX t0	NOP	SOP	SOP	SOP	SOP	SOP	COP	COP
TX	NOP	NOP	NOP	CR1	CR2	CR4	NOP	DB1
RX t1	NOP	CRX	CR4	FC	FC	NOP	DB1	NOP
TX	NOP	NOP	NOP	...	...	CR3	NOP	DB2
RX t2	NOP	FC	CR3			NOP	DB2	NOP
TX	NOP	...	NOP			CR2	NOP	DB3
RX t3	NOP		CR2			NOP	...	...
TX	NOP	...	NOP			CR1	...	...
RX t4	NOP	...	CR1			FC	DB7	NOP
TX	NOP		NOP			...	NOP	DB8
RX	NOP		FC				DB8	FC

5. ARCOFI ELECTRICAL CHARACTERISTICS

The following section define the electrical characteristics of the ARCOFI under normal operating conditions unless otherwise specified.

Vdd = 5V +/- 5% , DGND = OV
Vss = -5V =/- 5%
TEMP = -25 to 70 C

5.1 ABSOLUTE MAXIMUM RATING

	SYMBOL	MIN	MAX	UNIT
Storage temperature	Tstg	-60	125	C
Ambient temperature under bias	Ta	-30	80	C
Vdd referred to AGND		-0.3	5.5	V
Vss referred to AGND		-5.5	0.3	V
AGND to DGND		-0.3	+0.3	V
Analog input and output voltages	V			
referred to Vdd		-11	+0.3	V
referred to Vss		-0.3	+11	V
All digital input and output voltages	V			
referred to DGND		-0.3	-5.5	V
referred to Vdd		-5.5	0.3	V
Power dissipation	Pd		1	W

5.2 ARCOFI DC CHARACTERISTICS

DESCRIPTION	PARA-METER	CONDITION	MIN	MAX	UNIT
DIGITAL					
Input leakage Current	Iil	-0.3<=Vin<= Vdd		+/-10	uA
Input high level	Vih		2.4	Vdd+3	V
Input low level	Vil		-0.3	0.8	V
Output high level	Voh	Io = 400uA	2.4		V
Output low level	Vol	Io = -2mA		0.45	V
Vdd Supply current	Idd				
Standby		+/- 5% supply		2	mA
operating		+/- 5% supply		20	mA
Vss Supply current	Iss				
Standby *)		+/- 5% supply		0	mA
operating		+/- 5% supply		10	mA
Standby Power dissi-pation	Pdo	+/- 5% supply		10	mW
Operating power dis-sipation	Pdl	+/- 5% supply		150	mW
Input capacitance	Ci			10	pf
Output capacitance	Co			15	pf

*) With the AFE powered down

5.3 SLD Bus Switching Characteristics

DESCRIPTION	Parame-ter	MIN	MAX	UNIT
CK period	t(SCLK)	1.93	1.97	us
CK high pulse width	t(SCLKH)	800		ns
CK low pulse width	t(SCLKL)	800		ns
CK low to FSC high	t(CLKDU)	-400	400	ns
CK low to FSC low	t(CLKDD)	-400	400	ns
CK high t0 SIP in edge	t(DCLKSI)	0	400	ns
CK low to SIP in edge	t(CLKSI)	100		ns
SIP out tristate to FSC	t(DDTR)		50	ns
CK to SIP out	t(CLKSO)		200	ns

note: SIP is an I/O pin; SIP IN denotes timings for incoming data and SIP out denotes timings relation with out going data.

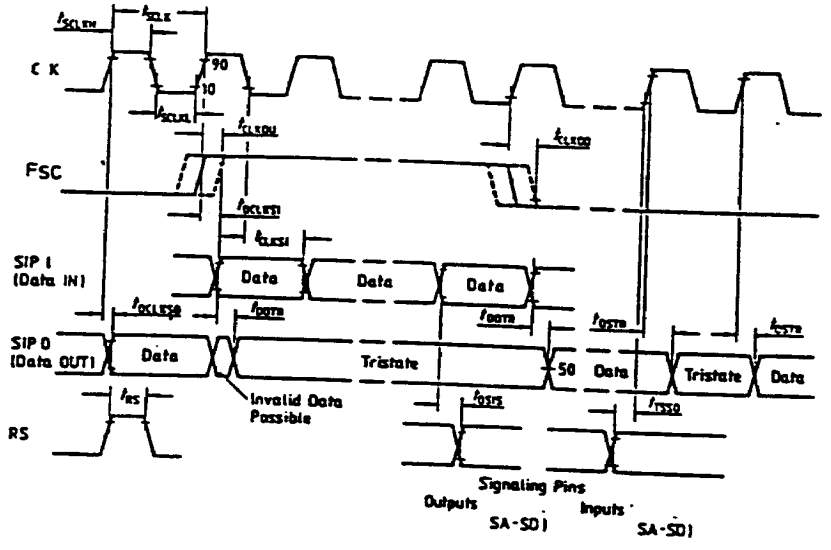
5.4 PCI Switching Characteristics

DESCRIPTION	Parame-ter	MIN	MAX	UNIT
SIP in to PCI out	t(DSIS)		200	ns
PCI in to CK	t(SSO)	50		ns

5.5 RESET TIMING

DESCRIPTION	Parame-ter	MIN	MAX	UNIT
Vdd rise time	t(RVdd)	0	20	ms
Reset pulse width	t(RS)	1		us
Power Stable to reset low	t(SRS)	1		us
Reset transition time	t(tr)		1	ms

5.4.1 PULSE DIAGRAM



5.5 PACKAGE OUTLINES